Cache retention time change method to reduce address resolution response time in wide area layer 2 network

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***Abstract*—In wide area Layer 2 (L2) networks, there is a problem that broadcast packets for address resolution fill up link capacities. As a result, address resolution using Address Resolution Protocol (ARP), which uses broadcasts, cannot be used in wide area L2 networks. A conventional research has proposed an architecture using Distributed Hash Table (DHT) and ARP cache for reducing broadcasts. However, since this architecture uses simple Least Recently Used (LRU) method for caching, some packets may be discarded because of continuous cache misses which require long address resolution response time. Therefore, we propose a cache retention time change method considering address resolution response time. In addition, we also propose cache insertion position determination methods based on several ideas. Finally, we evaluate the effectiveness of the proposed method.**

I. Introduction

In recent years, in order to respond to the rapidly increasing traffic and the diversification of communication services, the photonic L2 network attracts attention[1]. The aim of the photonic L2 network is providing various services and high-speed transmission with light paths on a common photonic L2. As one of the services, a wide area L2 network assuming a carrier network capable of accommodating one million users is considered. In wide area L2 networks, however, there is a problem that the broadcast packets occupy link capacities.

The broadcast reduction architecture in a wide area L2 network is proposed[2]. The architecture consists of edge nodes at the edges of the wide area L2 network and Software Defined Network (SDN) controllers managing one or more edge nodes without overlapping. Each edge node accommodates local area nodes and has ARP cache. The SDN controllers have ARP information of local area nodes and configure the DHT. The architecture tries to resolve an address according to the following priority. ①:The gateway edge node checks own ARP cache and sends an ARP reply, if possible. ②:The SDN controller responsible for the edge node checks the hash value of the destination IP address and the corresponding controller sends an ARP reply, if possible ③:The Architecture failing to resolve the address efficiently, all the edge nodes need to broadcast. The point to pay attention to here is that, in the architecture, all ARP information is managed by the DHT. Since which SDN controller maintains each ARP information is determined by the hashed value of the destination IP and not the destination IP itself, it can be assumed that ARP requests with large and small response times are uniformly generated. In the architecture, the LRU method is applied to the ARP cache and it deletes the least accessed ARP entry, meaning that the cache replacement is performed without considering the address resolution response time. As a result, if packets with destination IP that takes relatively longer to resolve arrive consecutively and cache misses accumulate, packet losses may occur due to buffer overflows.

II. Cache retention time change method

We propose a cache retention time change method. In this caching method, we set the cache partition space by changing the cache insertion position in accordance with the response time of address resolution. Figure 1 shows an example of the proposed method when the number of cache entries is 100 and there are three insertion positions. ARP information with a large response time is cached at a shallow position in the cache (position of entry 0), and similarly, small response time is cached at a deep position (position of entry 90). The operation in each partition space when and entry is cached is similar to FIFO, the last entry in each partition goes out to the next partition. When a cache hit occurs, the hit entry is deleted first and inserted into its original position. All entries from the original insertion position to the hit position are shifted one by one. By performing these operations, ARP entries are not deleted from the cache unless ones with equal or higher response time are cached. However, in the proposed method, cache performance is highly dependent on which ARP information is inserted at which position. Therefore, we propose cache insertion position determination methods based on several ideas.

A. Equal Expected Value (EEV)

As the first method, we propose a method to allocate so that the expected value of response time due to cache misses is equal for all response times. In this method, even if an ARP entry with the response time 2[msec] misses twice, it will not be a problem if the response time 4[msec] is found once. This idea can be written as, $2(1-\frac{A}{250}) = 4(1-\frac{B}{250}) \cdots (1)$. Figure 2 shows the example of this equation. In this example, we set the response time 2 to 5[msec] and for each response time, there are 250 destinations. The left-hand side of the equation is expected response time due to an address which takes 2[msec] for address resolution, and the right-hand side is that due to

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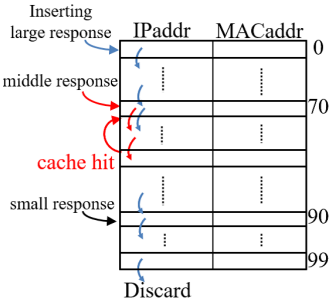

Fig. 1. example of cache retention time change method

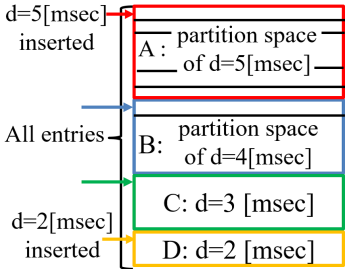

Fig. 2. example of EEV

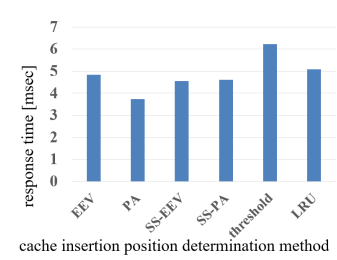

Fig. 3. Average response time of each caching method

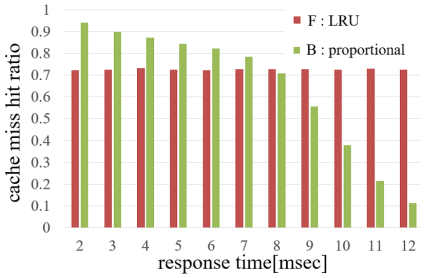

Fig. 4. relation of the response time and miss hit ratio

4[msec]. If there are more types in response times, similar equations need to be constructed for these ones as well. By solving the systems of these equations, we determine where each type of the addresses are inserted.

B. Proportional Allocation (PA)

As the second method, we propose a method to determine cache insertion position so that the cache partition space is proportional to the response time for address resolution. In this method, for example in Figure 2, cache partition space of $d = 4[msec]$ is twice that of $d = 2[msec]$. Cache partition spaces for all response times will be determined in this manner. As a result, the cache hit ratio becomes higher for destinations with larger response time.

C. Sheared Space EEV (SS-EEV)

In the methods described so far, It is assumed that the partition space of a response time is only used by the ARP information with its response time, and cannot be used by ARP information of other response times. However, in fact, a partition space with response time d can also use the partition spaces whose response time is less than d. For example, in Figure 2, last entry of space A goes out to the space B at next time. So space B will be shared between the two groups(each uses about $\frac{B}{2}$). Based on this idea, ARP information of $d = 4[msec]$ can use $\frac{D}{4} + \frac{C}{3} + \frac{B}{2}$. As a result, the equation of (1) will become $2(1 - \frac{\frac{D}{4}}{250}) = 4(1 - \frac{\frac{D}{4}+\frac{C}{3}+\frac{B}{2}}{250})$. Similar to EEV, a system of equations is established in this way, and appropriate cache insertion points are determined by solving it.

D. Shared Space PA (SS-PA)

Similar to SS-EEV, PA is modified so that the calculation takes into account the fact that cache partition space of response time d can also use ones that of shorter response times.

E. FIFO with threshold

In order to compare with other methods, we propose the method in which only ARP information with a response time above a threshold are cached. The operation is same as that of the FIFO which caches only ones above a threshold.

III. Simulation And Discussion

We set 1000 kinds of destinations of packets, and the response time of resolving a destination IP address is uniformly distributed from 2 to 12 msec. The number of entries of the cache is set 100, which is one tenth of the total number of destinations. The number of arrival packets is 10000. We compare the five cache insertion position determination methods explained before, with the normal LRU. The arrival packets have temporal locality; the probabilities that a packet with the same destination arrives again within 10 packets and 100 packets are 10% and 50%, respectively[3]. The average response time is shown in Figure 3. PA showed the best performance. It was 3.72[msec], and the LRU was 5.08[msec]. This shows that when the proposed methods are used and where ARP entries should be inserted is appropriately decided, it is possible to reduce the average response time by 1.36[msec](27%). In the Figure 4, proposed method with PA succeeds in reducing cache miss ratio for ARP request with response time 8[msec] or more has lower mishit ratio than LRU. We also confirmed reduction of cache miss ratio by about 60% for 12[msec], which is the destination with the longest response time. Although the cache miss ratio is high for ARP requests with short response time, it is not a problem because they are not accumulated in the packet buffer.

IV. Conclusion

In this paper, we solved the problem of packet loss due to the continuous packets with large address resolution time in the wide area L2 network. The conventional LRU method did not consider response time for address resolution. We proposed a cache method to changed the time held in the cache according to the response time. In addition, we also proposed several methods to decide where to insert an entry based of several ideas, and measured the performance of each. We reduced the cache miss rate of the destination with a large response time and confirmed the reduction of the average response time by the proposed scheme.

Acknowledgment

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References

[1] K. i. Kitayama, A. Hiramatsu, M. Fukui, T. Tsuritani, N. Yamanaka, S. Okamoto, M. Jinno, and M. Koga, "Photonic network vision 2020-toward smart photonic cloud," *Journal of Lightwave Technology*, vol. 32, no. 16, pp. 2760–2770, Aug 2014.

[2] Y. Nakajima, S. Okamoto, and N. Yamanaka, "Proposal of the scalable address resolution method in a photonic layer-2 network," *Journal of Lightwave Technology*, vol. 32, no. 16, pp. 2760–2770, 2014.

[3] M. H. M. W. Shi and P. Gburzynski, "Traffic locality characteristics in a parallel forwarding system," *INTERNATIONAL JOURNAL OF COMMUNICATION SYSTEM*, no. 16, pp. 823–839, June 2013.