A 10-Gb/s 4x2 CMOS/SIMOX Switch LSI for a 640Gb/s ATM Switching System

Yusuke Ohtomo, Eiji Oki and Naoaki Yamanaka
NTT

Outline

• Target and problems
• New scalable contention control
• Fully depleted SOI LSI design
• Performance
• Summary
Target

- 640-Gb/s ATM switching system
  - SW LSI count limits output link speed
  - one floor (2048 unit) -> one unit

Requirements for SW LSI:
- control cell contention in output line
- reduce SW LSI count;
- high-throughput (40 Gb/s / 2 chips)
- low power consumption (<10 W)

Conventional contention control

- Ring arbitration among switch LSIs must be completed within one ATM cell time.
The problem with ring arbitration

- output link speed limited by arbitration time

![Graph showing the relationship between number of row switch LSIs and maximum output link speed with arbitration delays of 1.0, 3.0, and 5.0 nanoseconds.]

Scalable Distributed Arbitration (SDA)

- ATM cells are transmitted via transit buffers to the output line.
- Arbitration is executed between output and transit buffers.
- Longest control signal transmission within one ATM cell time is between adjacent switch LSIs.
How do we select cells in two buffers?

1st selection rule
Select cell having earlier arrival time.

If equal arrival times:
2nd selection rule
Select k th output buffer, probability = 1/k
k th transit buffer, probability = (k-1) / k

Results: Keep fairness: total selection probability, 1/N

Fairness on ATM cell delay time

Number of switch LSIs \( N = 8 \)
Input line load 0.95

- Keep fairness wrt. delay time
- Reduce delay time

![Graph showing probability vs. cell time for different arbitration methods: Ring arbitration, SDA, with fairness and delay time comparison.](image-url)
Maximum ATM cell delay time

![Graph showing maximum ATM cell delay time](image)

- **Ring arbitration**
- **Reduction**
- **SDA**

The maximum delay time of SDA is not sensitive to \( N \).

Required output cell buffer size

![Graph showing required output cell buffer size](image)

- **ATM Cell loss ratio < 10^{-9}**
- **Ring arbitration**
- **Bottom switch LSI**
- **Top switch LSI**
- **SDA**

Buffer size reduction
Chip design

- 4x2 switch
- 10-Gb/s link
- SDA in BUFO
- FD-SOI
- design compatible
- Active-pullup I/O
- 1.25Gbps x 221pin

Fully depleted SOI device structure

S/D capacitance: 1/8, threshold voltage: 0.1 V lower than Vt(bulk)
Power reduction by using FD-SOI

- Same gate delay at 0.7 V lower VDD
- VDD: bulk vs SOI
  2.5 V  2.0 V

Power consumption: 36% reduction

Pseudo-ECL I/O circuits

- CMOS active-pullup (APU) I/O circuits
FD-SOI APU vs Conventional I/O

<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>APU</td>
<td>ECL</td>
</tr>
<tr>
<td>2Gbps</td>
<td>1.4 W</td>
</tr>
<tr>
<td>Standby</td>
<td>7 W</td>
</tr>
</tbody>
</table>

Input circuit: 105 pin  
Output circuit: 105 pin

Chip micrograph

- Switch size: 4 x 2
- Link speed: 10 Gb/s  
  (1.25 Gb/s x 8 parallel)
- Throughput: 40 Gb/s (2 chips)
- Architecture: SDA and TDXP
- Cell size: 64 B
- Technology: 0.25-μm CMOS/SIMOX
- Gate count: 288 k gates,  
  209-kb 2-port RAM
- I/O pin: In: 116, Out: 105
- Operating freq.: I/O: 1.25 Gb/s  
  Internal gates: 156 MHz
- Supply voltage: -2.0V, -1.3V (Vref)
- Die size: 16.55 x 16.55 mm²
- Power cons.: 7 W
Output waveforms

- Switch LSI functions at 200 MHz were confirmed with an LSI tester
- On-wafer speed measurement (at 1.25 Gb/s) to select chip mounting on an MCM

80-Gb/s ATM switching module

- 8 x 8 switch, 10 Gb/s/port
- Switch throughput: 80 Gb/s
- MCM
- Size: 114 x 160 mm
Summary

• 10-Gb/s 4x2 ATM switch LSI
  - Developed contention control, SDA
  • switch scalability
  - Fully depleted-SOI (CMOS/SIMOX)
  • 36% reduction in power consumption (11 W -> 7 W)
  - APU I/O circuit
  • 1.25-Gb/s, 221-pin pseudo ECL interface