switched. Both waves propagate forward along the CPW section. The COM is cut off (by placing metal planes very close to both sides of the dielectric substrate) at the appropriate distance from the diode plane. The CEM reaches the other end of the CPW section, being partially converted into COM forward and backward waves by the upper slot short-circuit. The COM forward-wave propagates out to the output slotline section. The COM backward-wave is cutoff at the appropriate distance. Modulator *S*-parameters and the phase-shift (both simulated using eqn. 3 and measured) are shown in Fig. 2*d*. Again, their agreement is excellent, demonstrating the validity of model and its applicability.

Conclusions: A new 'circuit model' that enables a quantitative analysis to be carried out of the energy exchange between even and odd modes at asymmetric shunt impedances in CPW, has been proposed, and applied to the simulation of CPW microwave circuits. The excellent agreement between simulated results and *S*-parameter measurements demonstrates the validity of the model and its usefulness as a CAD tool in the design and optimisation of hybrid/MMIC microwave CPW circuits.

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Scalable 10Gbit/s 4 × 2 0.25μm CMOS/SIMOX ATM switch LSI circuit based on distributed contention control

E. Oki, N. Yamanaka, K. Okazaki and Y. Ohtomo

A scalable 10Gbit/s 4 × 2 ATM switch LSI circuit has been fabricated. It employs a new distributed contention control technique that makes the LSI circuit expandable. To increase the LSI circuit throughput, 0.25μm CMOS/SIMOX (separation by implanted oxygen) technology is used. It allows the LSI circuit to offer 221 I/O pins, an operating speed of 1.25Gbit/s and 7W power consumption.

To meet the expected increase in demand for multimedia services, it will be necessary to create asynchronous transfer mode (ATM) switching systems that have a throughput of > 1Tbit/s. For such systems, an appropriate choice is the crosspoint-LSI-type switch architecture, in which identical switch LSI circuits are arranged on a matrix plane. The modularity of the switch design allows the switch to be easily expanded.

The conventional crosspoint-LSI-type switch architecture uses ring arbitration among switch LSI circuits to avoid output-bus-access contention, as shown in Fig. 1*a*. This contention occurs when ATM cells from different switch LSI circuits request transmission to the same output line (bus) during the same ATM cell time. The control signal for ring arbitration must pass through all the switch LSI circuits belonging to the same output line within the ATM cell time [1]. However, as the output-line speed increases, the ATM cell time decreases. In a crosspoint-LSI-type switch with a large number of row switch LSI circuits, ring arbitration cannot be completed within the short ATM cell time. Therefore, conventional switches based on ring arbitration are not scalable due to the centralised contention control mechanism. We have fabricated a scalable 10Gbit/s 4 × 2 switch LSI circuit that employs a new distributed contention control technique, called scalable distributed arbitration (SDA), that allows the LSI circuit to be expanded.

SDA has an ATM output buffer and a transit buffer at each output port in a switch LSI, as shown in Fig. 1*b*. An output buffer sends a request (REQ) to CNTL if there is at least one ATM cell stored in the output buffer. A transit buffer stores several cells that are sent from either the output buffer of the upper switch LSI or the transit buffer of an upper switch LSI circuit. The transit buffer also sends REQ to CNTL if there is at least one cell stored

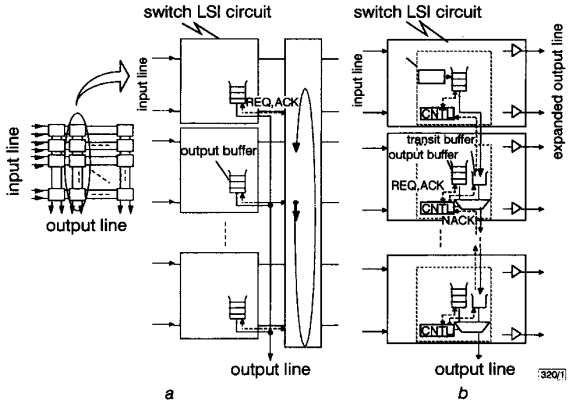

Fig. 1 *Contention control among switch LSIs*

a Ring arbitration (conventional)
b Scalable distributed arbitration (SDA) (proposed)

in the transit buffer. If the transit buffer is about to become full, it sends a not-acknowledgment (NACK) to the upper CNTL. If there is an REQ and CNTL does not receive NACK from the next lower transit buffer, then CNTL selects a cell within one ATM cell time. CNTL determines which cell should be sent according to its cell arrival time. To compare the arrival time of competing cells, we use a synchronous counter, which needs *S* bits. *S* was set to 8 in the switch LSI circuits. The selected ATM cell is transferred from its output buffer to the output line by way of several transit

buffers. The arbitration is executed in a distributed manner at each switch LSI circuit and the arbitration time does not depend on the number of connected switch LSI circuits. The longest control signal transmission distance for SDA within one ATM cell time is the distance between two adjacent LSI circuits.

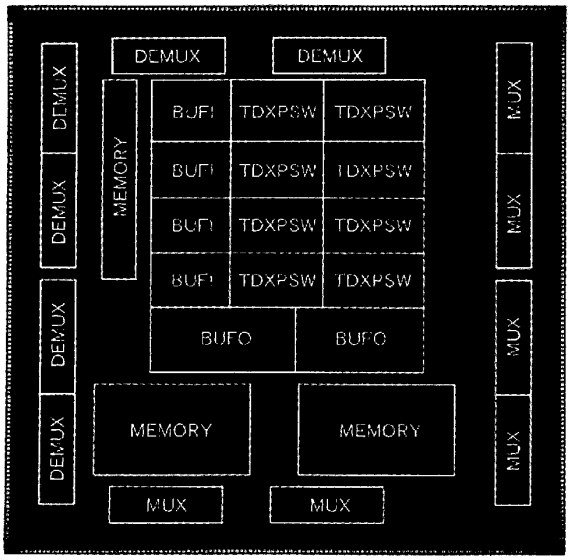

Fig. 2 *Chip micrograph*

Fig. 2 shows a microphotograph of the switch LSI circuit showing the function blocks. It has 288kgates and a 209kbit two-port RAM. The switch LSI circuit has a 4 × 2 switching function with input and output ATM link speed of 10Gbit/s. The switch LSI also has extended output ports to reduce input signal fanout. All input signals are transmitted via the switch LSI circuit in a pipelined manner. A 10Gbit/s ATM link is formed by eight single-ended I/Os at 1.25Gbit/s with an f/2 clock and frame signal, which are differential I/Os. The 1.25Gbit/s pseudo-ECL interface in the chip is constructed with CMOS low-voltage-swing I/O circuits, six 8:64 demultiplexers (DEMUX), and six 64:8 multiplexers (MUX) [2, 3]. The 10Gbit/s ATM cell stream is expanded to 64bits at an internal clock speed of 156MHz. An input/output-buffer-memory-type tandem-crosspoint switching architecture is employed in the switch LSI circuit [4]. The tandem crosspoint is implemented in TDXPSW. BUFI has a 16-cell ATM input buffer at each input port, and BUFO has a 128-cell ATM output buffer and a 16-cell transit buffer at each output port. These buffer memories are fabricated so as to hold the cell loss ratio to 10^{-9} under 0.9 offered load. The ATM cell size is 64 bytes. To support multicasting, 64 routing bits are used. SDA is implemented in BUFO. It reduces the operation speed for arbitration, compared to that for ring arbitration. The SDA operation is executed only between two adjacent LSI circuits within the ATM cell time of 51.2ns (eight internal clock cycles) in a pipeline manner. Since SDA uses cell selection control based on the ATM cell arrival time, the degree of ATM output buffering required is reduced by ~ 25%, compared with that of a switch LSI circuit using conventional ring arbitration. This is another advantage of SDA.

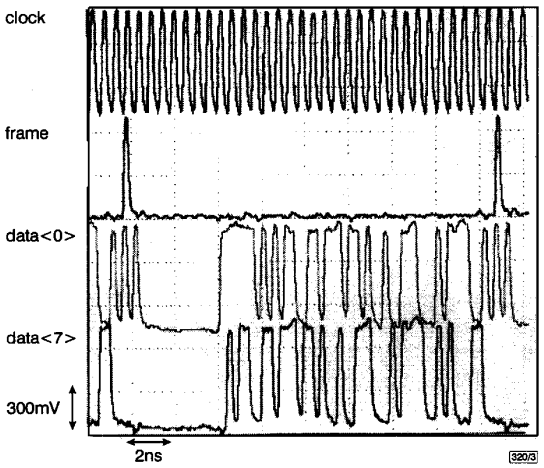

Fig. 3 *Measured output waveform at 1.25Gbit/s*

Table 1: Switch LSI specifications

Switch size	4 × 2
Link speed	10Gbit/s (1.25Gbit/s × 8 parallel)
Switch throughput	40Gbit/s (2 chips)
Priority class	Two
Cell size	64bytes
Total buffer size	360 cells
Technology	0.25μm CMOS/SIMOX
Gate count	288 kgates, 209kb 2-port RAM
I/O pin	In: 116, Out: 105
Operating frequency	I/O: 1.25Gbit/s Internal gates: 156MHz
Supply voltage	–2.0V, –1.3V (Vref)
Die size	16.55 × 16.55mm²
Power consumption	7W

All the switch LSI circuit functions were measured at the full required speed of 1.25Gbit/s as shown in Fig. 3, by using a build-up printed-wiring-board using flip-chip mounting. A power consumption of 7W is achieved by operating the CMOS/SIMOX gates at –2.0V. This consumption is 36% less than that of bulk CMOS gates (11W) at the same speed at –2.5V [5]. The specifications of the switch LSI are summarised in Table 1.

In conclusion, we have developed a 10Gbit/s 4 × 2 switch LSI circuit using 0.25μm CMOS/SIMOX technology. This chip employs a new distributed contention control technique that allows the LSI circuit to be expanded. The CMOS/SIMOX technology enables the LSI circuit to offer 221 pseudo-ECL pins at 1.25Gbit/s operating speed. In addition, a power consumption of 7W is achieved by operating the gates at –2.0V. The scalability offered by the switch LSI circuit is the key to multimedia terabit per second ATM switching systems.

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