Special care was taken with regard to data-to-clock phase alignment in the layout design. One of the differential signals in each demultiplexed channel is output, while the other is terminated with a 50Ω resistor in the IC chip. This is because of the restricted number of pads and lack of appropriate probes for on-wafer measurements. The chip is 2mm × 3mm in size and contains 379 active elements.

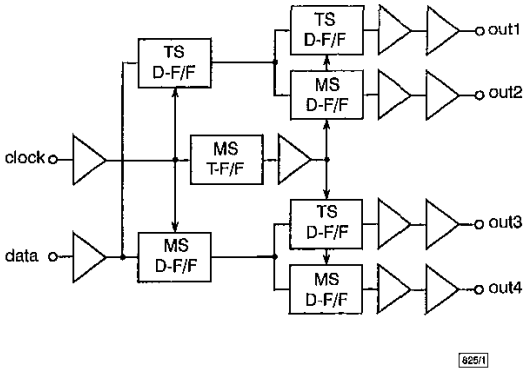

Fig. 1 *Block diagram of 1:4 demultiplexer IC*
MS: master-slave; TS: tri-stage

Fig. 2 *Measured eye diagrams of input and output for DEMUX IC*

Experimental results: The DEMUX IC was fabricated using reliable, non-self-aligned InP-based HBTs with a carbon-doped base and InGaAs/InP composite collector [5]. The HBTs had a unity current gain cutoff frequency (f_T) of 115GHz and a maximum oscillation frequency (f_{max}) of 154GHz at a collector current of 3mA and a collector-to-emitter voltage of 1.2V. These values are almost the same as those for HBTs previously presented by this group [5], which indicates good reproducibility in non-self-aligned HBTs. High-speed measurement of the DEMUX IC performance was carried out on-wafer with RF probes. A 40Gbit/s pseudorandom bit stream (PRBS) with a length of $2^{23} - 1$ was generated by quadruplexing 10Gbit/s, four-channel PRBSs in a 4:2 MUX and an HEMT 2:1 MUX [2], and then input to the DEMUX IC. Three out of the four channels from the DEMUX IC were monitored with a sampling oscilloscope; the other was input to an error detector. Fig. 2 shows the eye diagrams of the DEMUX IC input and output. The phase difference in the outputs is due to cable length differences. Error-free operation was confirmed with a phase margin of 100°. Power dissipation of the DEMUX IC was 2.97W at a supply voltage of –4.5V. Reducing the current in the 2:4 DEMUX part can decrease the consumption.

Conclusions: We have fabricated a 1:4 DEMUX IC using reliable, non-self-aligned InP-based HBTs with an f_T of 115GHz and an f_{max} of 154GHz. 40Gbit/s error-free operation with a phase margin of 100° was obtained. The power dissipation of the IC was 2.97W. This result indicates that InP-based HBTs are promising as high-speed, low-power lightwave communication ICs.

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Scalable frame-synchronisation circuit for highly parallel optical interconnections

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A scalable frame-synchronisation circuit is proposed for highly parallel high-speed optical interconnections. Its scalable architecture enables the number of channels to be increased without any decrease in the transmission rate. In HSPICE circuit simulations, a circuit using 0.25μm CMOS technology compensated for a skew in 622Mbit/s input data.

Introduction: Scalable architectures are often used for large asynchronous transfer mode (ATM) switching systems. The switching large scale integration (LSI) chips in the switch core are assembled into multi-chip modules (MCMs), which are interconnected. Deep sub-micrometre process technology has resulted in an increase in the switching speed of the core LSI chips, and the use of high-performance MCM technology has enabled these chips to be assembled into MCMs. The throughput of the interconnections in these MCMs must be high enough to prevent them from becoming a bottleneck. Instead of conventional electrical interconnections, parallel optical interconnections were used in a 100Gbit/s throughput ATM switch MCM [1, 2]. In the future, skew-compensation techniques such as bit-synchronisation and frame-synchronisation circuits for the received data will become important especially in highly parallel high-speed optical interconnections. We propose a frame-synchronisation circuit which has a scalable architecture that can handle highly parallel interconnections without any reduction in transmission rate.

Frame-synchronisation circuit: A frame-synchronisation circuit is normally used to (i) detect the frame-synchronisation pattern in each channel and (ii) count the offset clock cycles for each channel relative to the master channel. In a conventional circuit generating offset signals by comparing the phase of each channel with the master channel, a large propagation delay for the master channel prevents the offset signals from being properly generated when the number of channels is large.

We propose a scalable frame-synchronisation circuit that can handle interconnections with any number of channels. Fig. 1 shows a circuit that can be used to count offset clock cycles $c[i]$ for

n-channel parallel interconnections. This circuit operates in two steps. In the first step, the relative offset clock cycles between a pair of neighbouring channels is determined by comparing the phases of the frame-synchronisation-pattern detected signal $P[i-1]$ and $P[i]$. The number of relative offset clock cycles $d[i-1, i]$ is stored in the $(k+1)$ bit up/down counter in each channel. The most significant bit of the counter indicates a positive or negative bit and the initial values of all the counters are set to '0'. The counters are incremented by up/down enable signals synchronised to the transmission clock. The counter value varies from -2^k(111... 1) to 2^k-1 (011...1), where a negative value means that the ith channel has advanced ahead of the $i-1$th channel. In this step the circuit operates channel independently, so it can operate fast enough to synchronise the transfer rate for any number of channels.

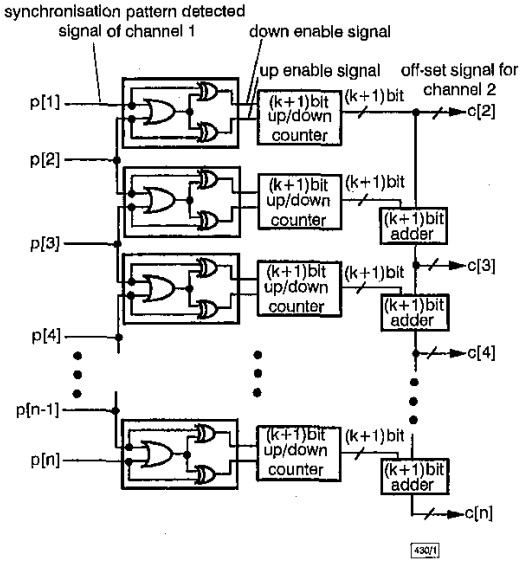

Fig. 1 *Proposed circuit for counting offset clock cycles*

In the second step, the offset clock cycles $d[i,1](2 \le i \le n)$ are calculated relative to the master channel (the channel number of which is assumed to be 1) by the following formula:

$$d[i,1] = d[i,i-1] + d[i-1,1] = \sum_{j=2}^{i} d[j,j-1] \quad (1)$$

This formula is executed by adders, as shown in Fig. 1, where $c[i] = d[i, 1]$ controls a selector to output the synchronised data from shift-registers containing the received serial data in each channel. The circuit operates channel independently in the first step and does not need to operate at high speed in the second step. Therefore, the maximum operating speed of the circuit is limited only by the first step so the number of channels can be increased without decreasing the transmission rate.

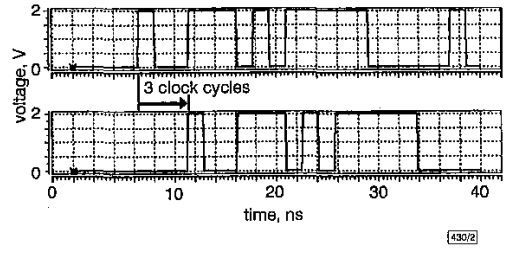

Fig. 2 *Skewed input signals for HSPICE simulation*

Circuit simulation: To estimate the efficiency of the proposed frame-synchronisation circuit, we performed HSPICE circuit simulation using 0.25μm CMOS device parameters. The bit-width of the counters and adders was four ($k = 3$) which means that the maximum number of clock cycles to be compensated for is seven ($2^3 - 1$) and the number of channels was eight. Fig. 2 shows the 622-Mbit/s input data of channels 1 (master) and 8 having a skew of three clock cycles. It was compensated for after the rising edge at 25.5ns, as shown in Fig. 3. Table 1 shows the circuit operation. We confirmed that the circuit could operate for any number of channels without decreasing the operating speed.

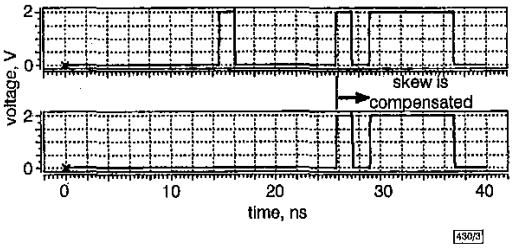

Fig. 3 *Simulated skew-compensated output signals*

Table 1: Example of circuit operation

Number of channels	Offset	Counter value	$c[i]$
1 (master)	–	–	–
2	–2	1110	1110
3	+3	0011	0001
4	–4	1100	1101
5	+5	0101	0010
6	–3	1101	1111
7	–3	1101	1100
8	+7	0111	0011

Conclusion: A scalable frame-synchronisation circuit has been proposed for highly parallel high-speed parallel optical interconnections. This circuit can be used to count offset clock cycles by using a channel-independent architecture. Therefore, it can handle interconnections with any number of channels without decreasing the transmission rate. A circuit simulated by HSPICE with 0.25μm CMOS device parameters, was able to compensate for a maximum of seven clock cycles of skew in 622Mbit/s input signals.

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