A 100-Gb/s Throughput ATM Switch MCM with a 320-Channel Parallel Optical I/O Interface

Ryusuke Kawano, *Member, IEEE*, Naoaki Yamanaka, *Fellow, IEEE*, Eiji Oki, *Member, IEEE*, Seisho Yasukawa, *Member, IEEE*, Katsuhiko Okazaki, Akira Ohki, Mitsuo Usui, Nobuo Sato, Kosuke Katsura, *Member, IEEE*, Yasuhiro Ando, *Senior Member, IEEE*, Toshiaki Kagawa, and Makoto Hikita, *Member, IEEE*

***Abstract*—For an ATM switch system, we have developed a 100-Gb/s input/output (I/O) throughput optical I/O interface ATM switch multichip module (MCM) that has 320-ch optical I/O ports. This MCM is fabricated using ceramic (MCM-C) technology and very-small highly-parallel O/E and E/O optical converters. It uses 0.25-μm complementary metal oxide semiconductors (CMOS) ATM switch large scale integrations (LSIs) and has a total I/O throughput of up to 160 Gb/s. A prototype module with total I/O throughput of 100 Gb/s has been partially assembled using eight optical I/O interface blocks, each composed of a 40-ch O/E converter and a 40-ch E/O converter; the data rate per channel is from dc to 700 Mb/s. Using this module we developed an optical I/O interface ATM switch system and confirmed the operation of the optical interface.**

***Index Terms*—ATM, MCM, optical I/O MCM, parallel optical interconnection, wiring bottleneck.**

I. INTRODUCTION

TRAFFIC speeds and volumes are expected to increase as a result of demand for high-speed multimedia services. Technological progress is needed from the transmission layer, such as optical fibers, to the application layer, such as electronic commerce, to support a platform that can handle the increasing amount of information in circulation. The development of a high-speed and large-capacity switching node system is one step and a Tb/s class ATM (asynchronous transfer mode) switching system, which is suitable for handling multimedia, is under research and development, for example [1]–[3]. The core of the high-speed and large-capacity ATM switching system, that is, the routing-block, is constructed from some switching modules that are composed of switching LSIs. The quantity of hardware necessary for a Tb/s ATM switch system will be very large unless the core's switching modules are made as small as possible. A key technology for miniaturizing the switching module is the fine process technology of LSI. The number of functions in a chip has steadily increased and the I/O speed of switching LSIs has reached the Gb/s level. However, this rapid progress of LSI technology has led to difficulties in assembling such LSIs on a printed circuit board (PCB) from the viewpoints of high-speed and highly-parallel transmission, electrical power supply, area for termination resistors, and cooling. Thus, high-performance switching LSI assembly itself has been a bottleneck in the development of the switching core. Therefore, we have developed an "optical I/O interface ATM switch MCM," which is composed of an 80-Gb/s electrical MCM ATM switch block using MCM-C technology and a 40-ch E/O and O/E conversion parallel optical I/O interface block. A prototype using eight optical I/O interface blocks, whose total throughput is 100 Gb/s, has been assembled and tested, confirming successful optical input and output operation of the module. This paper describes the concept of the optical I/O interface ATM switch MCM, its fabrication, and its use in developing an optical I/O interface ATM switch system, and presents some measured results.

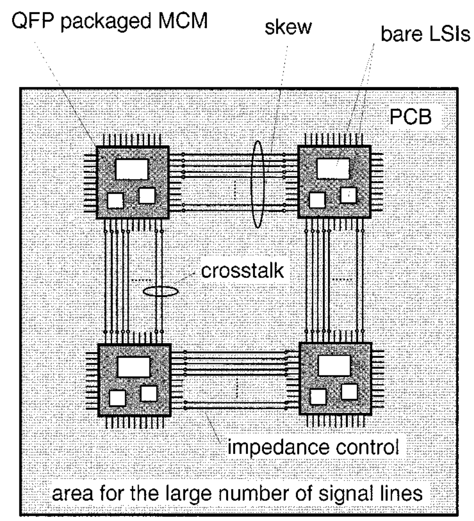

Fig. 1. Conventional module-to-module interconnection.

II. CONCEPT OF THE OPTICAL I/O INTERFACE MCM

For fabricating a high-throughput ATM switch module, it would be useful if we could raise the I/O pin speed of the LSI since that would suppress the required pin count of switching LSIs, which is now increasing due to the accumulation of functions made possible by the fine process technology of LSI. In fact, a CMOS switch LSI having an I/O speed of 1.25 Gb/s per pin [4] and a 4:1 MUX circuit with 2.6-Gb/s/pin I/O [5] have been developed. Although assembling packaged LSIs on a PCB may be effective if the LSI I/O signal speed is under about

Manuscript received June 4, 1999; revised September 27, 1999. This work was presented at the IEEE 49th Electronic Components and Technology Conference, San Diego, CA, June 1–4, 1999.

The authors are with the Ultra-High-Speed Module Division, Nippon Telegraph and Telephone Corporation, Kanagawa Prefecture 243-0032, Japan.

Publisher Item Identifier S 1521-3323(01)02417-0.

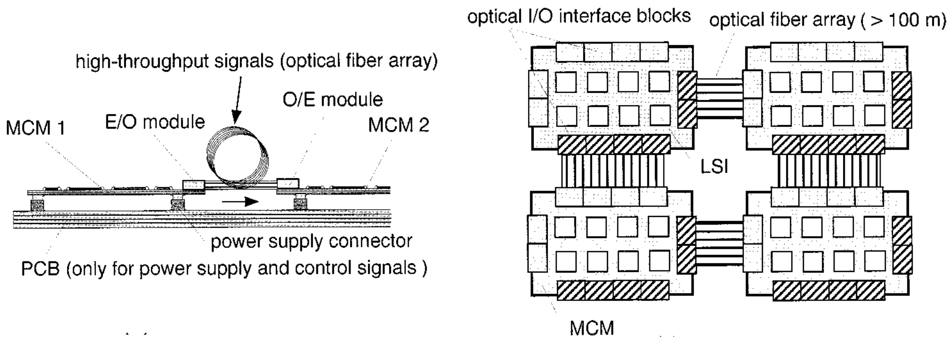

Fig. 2. Concept of the optical I/O interface MCM.

600 Mb/s, it may be difficult to use wiring for highly-parallel I/O signals above 1 Gb/s from the viewpoints of transmission characteristics and skew. Therefore, the problem has been how to assemble an LSI having parallel high-speed interconnections. To meet these requirements, an ATM switch module using MCM has been developed, for example, an 80-Gb/s ATM switching module, which has total I/O throughput of 160-Gb/s, using ceramic 40-layer MCM-C technology [6]. Although ceramic MCM-C technology allows miniaturization and high-speed chip-to-chip interconnection, it only moves the boundary of the high-throughput region from the LSI to the MCM. Therefore, MCM-to-MCM (module-to-module) interconnection will be a bottleneck if the I/O speed of MCMs goes beyond 1 Gb/s, because conventional MCM-to-MCM interconnection had been attained by signal lines in a PCB as shown in Fig. 1. If the medium for the high-speed and highly-parallel signal transmission is a PCB, then the transmission length and flexibility will be limited. Moreover, it will be difficult to control the signal line length, to suppress skew, and the impedance; ensure a sufficient area for a large number of signal lines; and suppress crosstalk. These days, research and development of parallel optical interconnection modules are being actively undertaken [7]–[10]. We believe that the best solution for versatile interconnection of MCMs is for an MCM to have its own built-in optical I/O interface using a parallel optical interconnection module. For this purpose, we propose the concept of an "optical I/O interface ATM switch MCM," which is shown in Fig. 2. The ATM switch module contains O/E and E/O modules inside it and the input and output to and from it is done only by optical signals. In the configuration of the optical I/O interface MCM, the PCB is used only for power supply and control signals. In other word, electrical parallel signal interconnections in the PCB have been eliminated. This work has extended the frontiers of the optical interface in the assembly layer of a high-throughput switch system as shown in Table I.

III. Module Structure

The composition of the developed optical I/O interface ATM switch MCM is shown in Fig. 3. It has three main parts: an 80-Gb/s electrical MCM ATM switch block using MCM-C technology, a 40-ch optical I/O interface block, and a metal frame with a liquid cooling jacket. These parts are described in detail in Section III-A—III-C, respectively. There are two kinds of optical I/O interface block for E/O and O/E conversion. Each block has 40 channels, so with eight converters, the optical I/O ports have a total of 320 channels. This structure keeps the electrical wiring as short as possible and completely eliminates it from the PCB; the switching module itself has only optical I/Os.

TABLE I
Assembly Layer and Optical Interfaced

	conventional media	introduction of optical interface
Rack-to-rack	cable	↓
Unit-to-unit	cable	↓
Board-to-board	backplane	↓
Module-to-module	PCB	this work
Chip-to-chip	PCB or ceramic	⋮
Gate-to-gate	metal line	↓

A. 80-Gb/s MCM ATM Switch Block

The 80-Gb/s MCM ATM switch is block A in Fig. 3. It is an 8×8 ATM switching MCM having switch throughput of 80 Gb/s using 40-layer ceramic MCM technology. This module is 114 mm $\times$ 160 mm. Eight switch LSIs and MCM-interface LSIs are mounted on the MCM substrate. The switch LSIs are fabricated by 0.25-μm CMOS/separation by implanted oxygen (SIMOX) devices [11]. The switch LSI provides 4×2 switching, handling input and output line speeds of 10 Gb/s. To reduce the number of high-speed I/O pins and achieve high throughput, we constructed the Gb/s I/O interface using CMOS low-voltage-swing I/O circuits [5]. A 10-Gb/s-cell stream is transmitted by eight physical lines at 1.25 Gb/s each. The MCM-interface LSIs were fabricated from high-speed Si-bipolar devices using super-self aligned process technology SST-1B [12].

They have serial-to-parallel and parallel-to-serial conversion functions to convert the line speed between the 16 physical lines at 625 Mb/s and eight physical lines at 1.25 Gb/s. This MCM has several features: the internal signal transmission speed is 1.25 Gb/s on the MCM and the interface speed is 625 Mb/s; termination resistors were fabricated by thin film processes and their size is very small; there are many power supply layers, whose impedances are reduced by 50-μm ceramic-sheet layers.

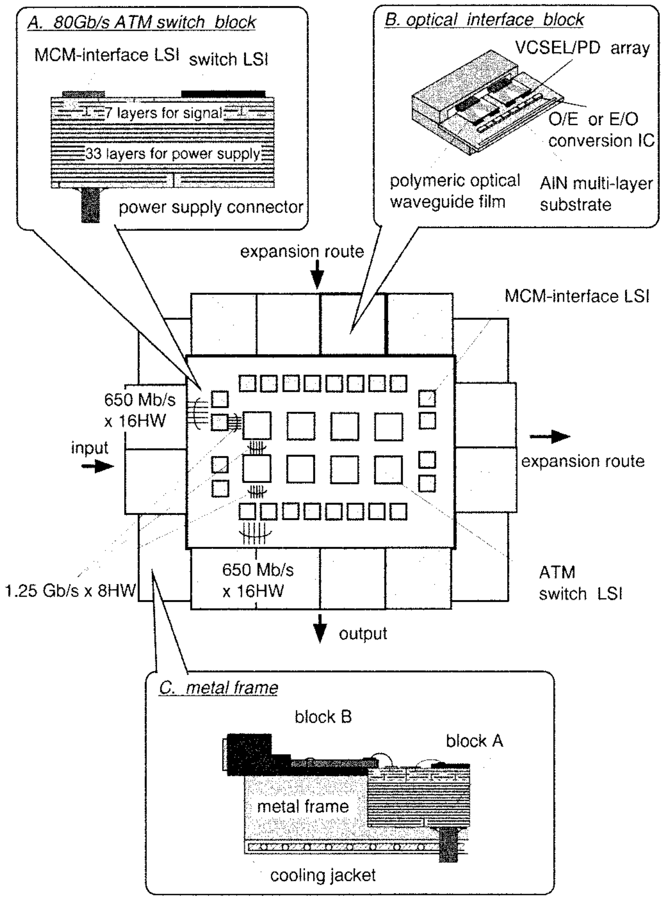

Fig. 3. Structure of the optical I/O interface MCM.

B. Optical I/O Interface Block

The optical I/O interface is block B in Fig. 3. This block is a parallel optical module called ParaBIT, for parallel inter-board optical interconnection technology [7]. The module has a simple structure which allows O/E and E/O operation without any multiplexor, demultiplexor, or retiming circuits, and uses simple electronic circuits with a fixed-decision-level receiver and an APC-less (APC: automatic power control) transmitter for low cost and low power consumption. The transmitter module consists of four 10-ch vertical cavity surface emitting laser (VCSEL) arrays, eight 5-ch TX-ICs, two 20-ch polymeric optical waveguide films with 45° mirrors, and two 20-fiber bare fiber (BF) connector receptacles. The receiver module consists of four 10-ch PD arrays, eight 5-ch RX-ICs, two 20-ch polymeric optical waveguide films with 45° mirrors, and two 20-fiber BF connector receptacles. Including losses at the 45° mirror and BF connectors, the average insertion losses of the coupling components for TX and RX were 2.3 and 2.2 dB, respectively [13]. Multimode optical fiber ribbons (graded index 50/125 μm: GI-50/125) are used for the interconnect. The total skew of the optical I/O interface block is about 240 ps including the 10 m fiber ribbons. 10-ch VCSEL arrays are used for the optical signal sources. A skew due to the laser operation delays of these VCSELs is negligible because these VCSELs are dc-biased above the threshold currents. Then the total Tx skew that includes the skew of the 10 m-long multimode fiber ribbons is less than 80 ps. In regard to the Rx modules, the skew that is induced by the intensity variation of incident optical signals is dominant because the fixed-decision-level type receivers ICs are used in the Rx module. We suppress the intensity variation of incident optical signals to be less than 2 dB by using the highly uniform VCSEL arrays. This 2 dB variation corresponds to the Rx skew of about 160 ps. Thus we achieve that the total skew of the optical I/O interface block is less than 240 ps. The above components are mounted on an AlN multilayer substrate that is 39 mm wide, 17 mm long, and 1 mm thick attached to a 150-μm pitch electrical I/O wire-bonding pad with a ground-signal-ground structure. The E/O (TX) and O/E (RX) modules are only 39 $\times$ 35 $\times$ 6.5 mm each as a result of high-density assembly of parts and the maximum deviation of their electrical signal length is less than 2 mm, which corresponds to skew of 13 ps.

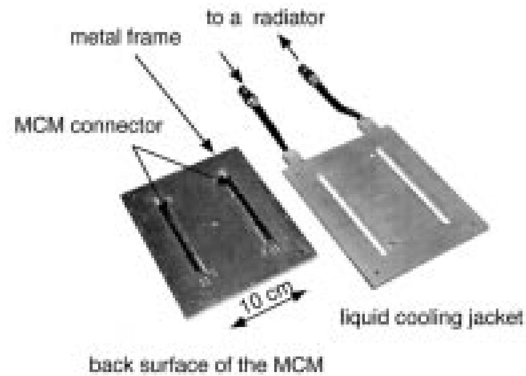

Fig. 4. Photograph of the liquid cooling jacket.

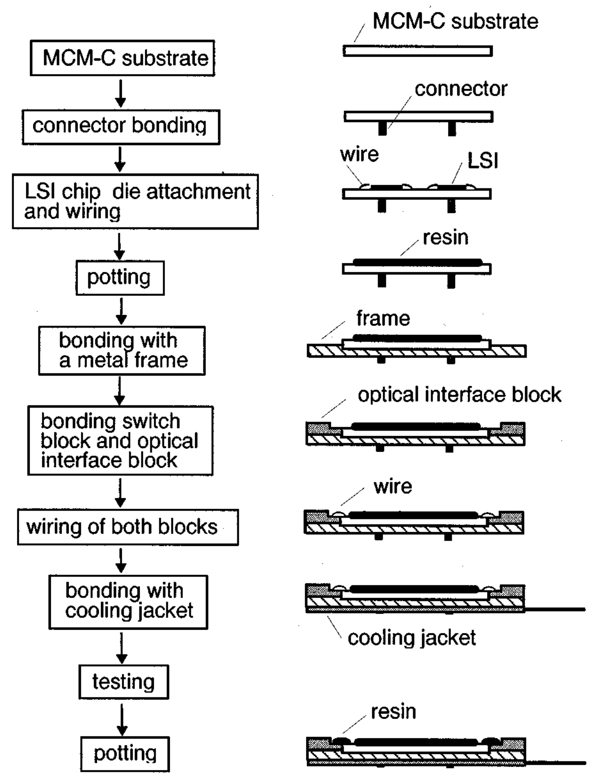

Fig. 5. Fabrication process of the module.

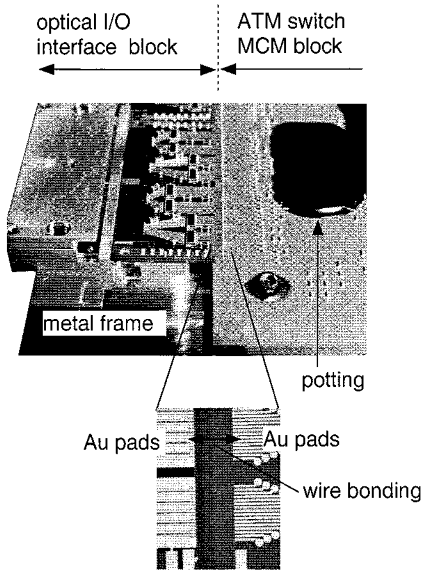

Fig. 6. Au wire-bonding pad configuration of each block.

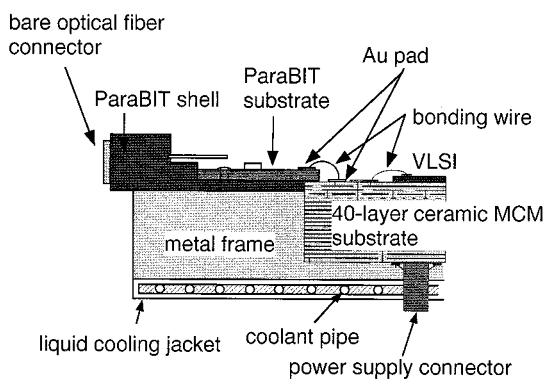

Fig. 7. Details of connections in each block.

C. Cooling Structure

The liquid cooling jacket and the 80-Gb/s electrical MCM ATM switch combined with the metal frame are block C in Fig. 3. A photograph of the jacket is shown in Fig. 4. The jacket has a coolant pipe inside it and the connector, which sticks out from the jacket, is connected to a distant radiator. The cooling performance of the jacket was precisely measured using a heater block. The thermal-resistance of the jacket was 0.082 °C/W.

IV. Fabrication Process

A. Total Module

Fig. 5 shows the fabrication process of the module. First, an MCM-C substrate for the MCM ATM switch block is fabricated and the condition of its electrical paths is evaluated. Then, the MCM-connector for power supply and control signals is bonded to the MCM. After LSI chip die attachment and wiring of the LSIs on the MCM, the bare LSIs are encapsulated in resin (potting) to protect their bonding wires and surfaces. Next, the MCM ATM switch block and a metal frame are bonded using conductive paste. The optical interface block is also bonded using conductive paste. Au bonding pads built into both the ATM switch block and the optical I/O interface block are arranged face-to-face, as shown in Fig. 6, and are connected electrically by wire bonding. Finally, a liquid cooling jacket is attached and tested. After correct operation has been verified, the wires between the switch block and the optical I/O interface are encapsulated in resin (potting). Fig. 7 shows details of the connections of each block. A metal frame is placed around the MCM ATM switch block, and optical I/O interface blocks are mounted on the frame. The shell of the optical module has a fiber connector

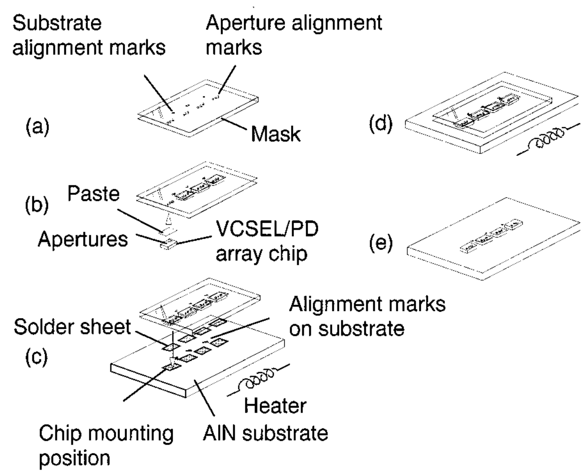

Fig. 8. TMB process.

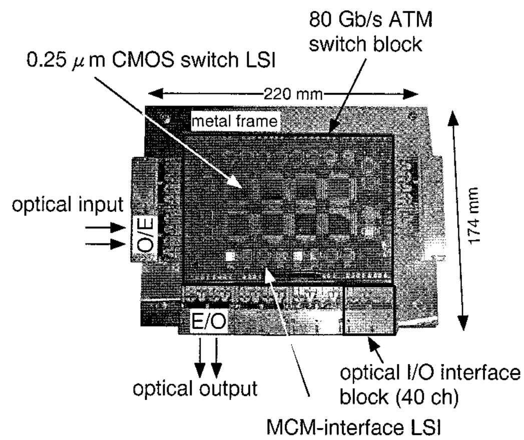

Fig. 9. Photograph of the module.

TABLE II
MAIN FEATURES OF THE MODULE

Switch throughput	80 Gb/s
Total I/O throughput	up to 160 Gb/s
ATM-cell link speed	10 Gb/s (625 Mb/s x 16)
I/O interface	parallel optical link
Data rate/ch of I/O	625 Mb/s
Light source	VCSEL array (850 nm)
I/O length	> 100 m
Module dimensions	220(L) x 174(W) x 15(H) mm
Power dessipation	266 W (including I/O interface part)
Cooling	liquid cooling

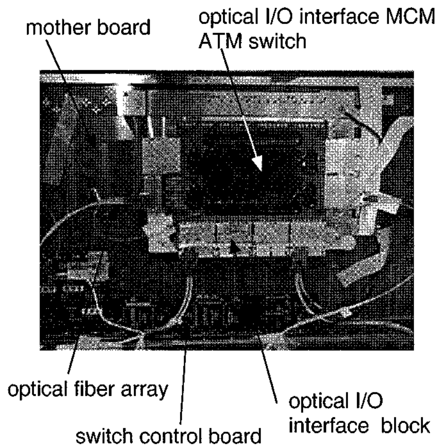

Fig. 10. Optical I/O MCM mounted in the unit.

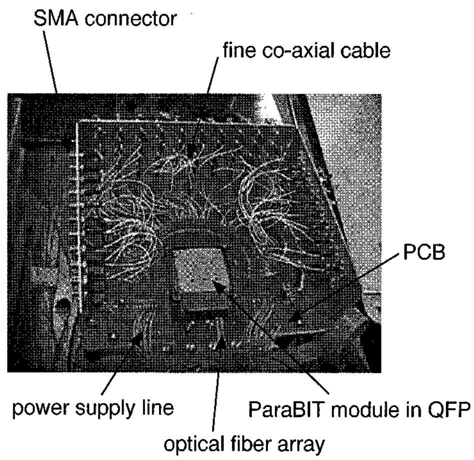

Fig. 11. E/O converter for system evaluation.

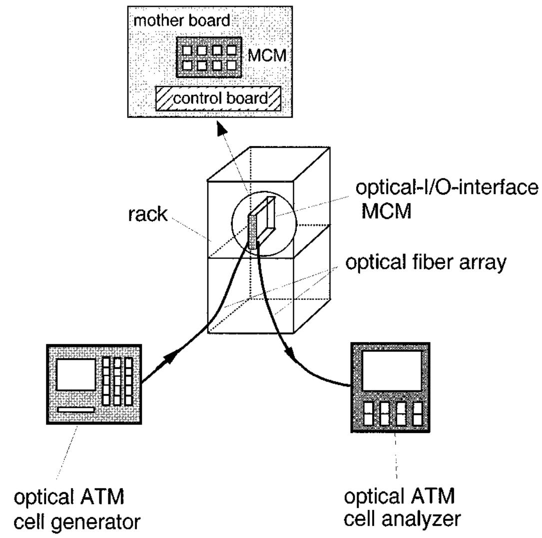

Fig. 12. System for evaluating optical I/O MCM.

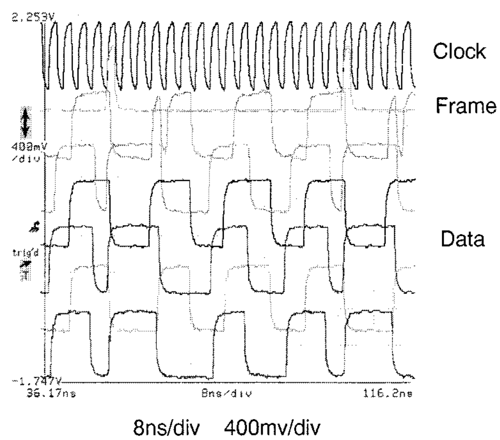

Fig. 13. Operating waveforms of optical I/O MCM (at 625 Mb/s).

enabling optical fibers to be slipped on and off. The optical I/O interface MCM is cooled by a liquid cooling jacket.

B. Optical Interface Block

In the optical interface block fabrication, multiple optical array chips, such as VCSEL/PD arrays, are mounted on an AlN substrate, and those chips are coupled to the waveguides through the 45° mirror by passive optical alignment. Obtaining the maximum optical coupling efficiency at the E/O and O/E interfaces requires positioning and diebonding the optical array devices precisely on the designed position. And all array device chips must be mounted simultaneously to shorten the exposure of the optical devices to high temperature (higher than the melting point of solder), to avoid damaging the device. Transferred multichip bonding (TMB) is being developed to satisfy the above requirements for multichip diebonding. The process of this technique in the fabrication of optical interface block (Fig. 8) is described as follows.

1) A quartz plate with aperture alignment marks and substrate alignment marks, representing the precise relative position of apertures on the four VCSEL/PD array chips and the designed location of chips on the four VCSEL/PD array chips and the designed location of chips on the AlN substrate, is prepared [Fig. 8(a)]. We call this quartz plate the “mask.” The apertures mean individual light-emitting elements on the VCSEL array or individual photo-detecting elements on the PD arrays.
2) Each chip is stuck, using paste, after each aperture on the chip is aligned face to face the aperture alignment mark on the mask using a microscope [Fig. 8(b)].
3) The AlN substrate is heated above the melting point of the solder sheet. The substrate alignment marks of the mask are aligned onto alignment marks formed on the AlN substrate [Fig. 8(c)]. The chips attached to the AlN substrate are kept in contact with the mask for short time [within 1 min; Fig. 8(d)].
4) After cooling, the AlN substrate is separated from the mask. As a result, the four VCSEL/PD array chips are transferred from the mask to the AlN substrate and simultaneously diebonding exactly onto the desired position [Fig. 8(e)]. Last, the paste on the chips and mask is cleaned using organic solvents.

A photograph of the optical I/O interface ATM switch MCM is shown in Fig. 9 and it main features are summarized in Table II.

V. Development of Optical I/O Interface ATM Switch System

Besides the optical I/O interface ATM switch MCM, we also developed a power supply system, rack, mother-board on which the ATM switch MCM and its control board are mounted, and a liquid cooling system. Evaluations of the optical I/O interface ATM switch MCM were performed on the unit shown in Fig. 10. The power supply voltage and control signals to the optical I/O interface ATM switch MCM are supplied via the connector on the back of the MCM. As the MCM only has an optical I/O interface, we had to generate 20-ch parallel optical signals from an electrical multichannel pulse pattern generator (PPG) for signal input to the MCM. We also had to convert the 20-ch optical output signals to electrical signals in order to analyze them with an electrical oscilloscope. Therefore, we also developed a device that converts the electrical multichannel PPG signal into parallel optical signals and a device that converts the optical MCM output into electrical parallel signals, as shown in Fig. 11. The E/O and O/E converters have the same outlet. The main components of these two devices are ParaBIT modules, which are assembled in QFP packages. The entire system is shown in Fig. 12.

VI. Evaluation Results

The 10 Gb/s optical ATM cell was put into the input port of the optical I/O interface ATM switch MCM and that was taken from the output port after routing. This indicates speed and skew performance is successfully implemented as the design. Fig. 13 is the example output waveform of the clock, frame and the 625 Mb/s signals of the one link. The one link speed is 10 Gb/s and the link is constructed of sixteen 625 Mb/s signals. In the Fig. 13, six of 625 Mb/s signals are shown. This is just because of the limitation of the display of the oscilloscope. The correct operation is confirmed by changing the monitor signals in sequence.

VII. Conclusion

We have developed an optical I/O interface ATM switch MCM. The module has only an optical interface for signal interconnection. For the optical interface, we used a parallel optical interconnection module which offers a smaller size and cost. The channel speed is 625 Mb/s and the total I/O throughput of the MCM is up to 160 Gb/s. A prototype module has been partially assembled with eight optical I/O interface blocks each having 40 channels. Using it we constructed an optical I/O interface ATM switch system and confirmed successful operation of the optical I/O interface.

References

[1] N. Yamanaka, S. Yasukawa, E. Oki, and T. Kawamura, "OPTIMA: TB/S ATM switching system architecture: Based on highly statistical optical WDM interconnection," in *Proc. ISS'97*, 1997, pp. 255–260.

[2] K. Y. Eng, M. J. Karol, G. J. Cry, and M. A. Pashan, "Design and prototype of a terabit ATM switch using a concentrator-based growable switch architecture," in *Proc. ISS'95*, 1995, pp. 404–408.

[3] E. Munter, J. Parker, and P. Kirkby, "A high capacity ATM switch based on advanced electronic and optical technologies," in *Proc. ISS'95*, 1995, pp. 389–393.

[4] E. Oki, N. Yamanaka, and Y. Ohtomo, "A 10 Gb/s (1.25Gb/s×8) 4×2 CMOS/SIMOX ATM switch," in *Proc. ISSCC Dig. Tech. Papers*, 1999, TA 9.6, pp. 170–172.

[5] Y. Ohtomo, S. Yasuda, M. Nogawa, J. Inoue, and M. Ino, "A 2.6 Gbps/pin CMOS/SIMOX low-voltage-swing interface circuit," *IEICE Trans. Electron.*, vol. E79-C, no. 4, pp. 524–529, Apr. 1996.

[6] E. Oki, N. Yamanaka, S. Yasukawa, R. Kawano, and K. Okazaki, "Merging advanced electronic and optical WDM technologies for 640-Gbit/s ATM switching system," in *Proc. ICC Dig. Tech. Papers*, 2000.

[7] K. Katsura, M. Usui, N. Sato, A. Ohki, N. Tanaka, N. Matsuura, T. Kagawa, K. Tateno, M. Hikita, R. Yoshimura, and Y. Ando, "Packaging for a 40-channel parallel optical interconnection module with an over-25-Gb/s throughput," in *Proc. 48th Electron. Comp. Technol. Conf.*, 1998, pp. 755–761.

[8] H. Karstensen *et al.*, "Parallel optical link (PAROLI) for multichannel gigabit rate interconnections," in *Proc. 48th Electron. Comp. Technol. Conf.*, 1998, pp. 747–754.

[9] L. J. Norton *et al.*, "OPTOBUSI™: A production parallel fiber optical interconnect," in *Proc. 47th Electron. Comp. Technol. Conf.*, 1997, pp. 204–209.

[10] A. Miura *et al.*, "Reliable, compact, CMOS interface, 200-Mbit/s x 12-channel optical interconnects using single-mode fiber arrays," in *Proc. 47th Electron. Comp. Technol. Conf.*, 1997, pp. 225–230.

[11] Y. Ohtomo, S. Yasuda, M. Nogawa, J. Inoue, K. Yamakoshi, H. Sawada, M. Ino, S. Hino, Y. Sato, Y. Takei, T. Watanabe, and K. Takeya, "A 40 Gb/s 8x8 ATM Switch LSI using 0.25m CMOS/SIMOX," in *Proc. ISSCC'97*, 1997, FA 9.3, pp. 154–155.

[12] T. Sakai, S. Konaka, Y. Kobayashi, M. Suzuki, and Y. Kawai, "Gigabit logic bipolar technology: advanced super self-aligned process technology," *Electron. Lett.*, vol. 19, pp. 283–234, 1983.

[13] M. Usui, M. Hikita, R. Yoshimura, N. Matsuura, N. Sato, A. Ohki, T. Kagawa, K. Tateno, K. Katsura, and Y. Ando, "An optical coupling technique for parallel optical interconnection modules using polymeric optical waveguide films," in *Proc. 1998 IEMT/IMC Symp.*, 1998, pp. 127–132.

Ryusuke Kawano (M'98) was born in Oita, Japan, on April 2, 1964. He received the B.E. and M.E. degrees from the University of Osaka Prefecture, Japan, in 1987 and 1989, respectively.

In 1989, he joined Nippon Telegraph and Telephone Corporation (NTT), Kanagawa Prefecture, Japan, and began researching and developing process technology for high-speed Si-bipolar devices. Since 1992, he has been engaged in researching and developing high-speed integrated circuits using Si bipolar transistors and GaAs MESFETs at the NTT LSI Laboratories, Kanagawa. After moving to NTT Network Service Systems Laboratories, Tokyo, Japan, his current research interests includes very large capacity ATM switching hardware such as high-speed logic, optical interconnection, and cooling.

Mr. Kawano is a member of the IEICE of Japan.

Naoaki Yamanaka (F'00) was born in Sendai City, Japan, on July 22, 1958. He received the B.E., M.E., and Ph.D. degrees in engineering from Keio University, Japan, in 1981, 1983, and 1991, respectively.

In 1983, he joined the Communication Switching Laboratories, Nippon Telegraph and Telephone Corporation (NTT), Tokyo, Japan, where he was engaged in research and development of a high-speed switching system and high-speed switching technologies such as ultra-high-speed switching LSI, packaging techniques, and interconnection techniques for Broadband ISDN services. Since 1989, he has been active in the development of Broadband ISDN based on ATM techniques. He is now researching future ATM based broadband ISDN architecture, and traffic management and performance analysis of ATM networks. He is currently a Senior Research Scientist, Supervisor, Research Group Leader in Mega-media Network System Project, Network Service Systems Laboratories, NTT. He is Associate Editor of the *IEICE Transactions on Communications*.

Dr. Yamanaka received Best of Conference Awards from the 40th, 44th, and 48th IEEE Electronic Components and Technology Conference, in 1990, 1994, and 1998, respectively, the TELECOM System Technology Prize from the Telecommunications Advancement Foundation, and the Best Transaction Paper Award from IEEE CPMT, in 1995 and 1996, respectively. He is a member of the Institute of Electronics, Information, and Communication Engineers (IEICE) of Japan. He is Broadband Area Editor of the *IEEE Communication Surveys* and TAC Chair of the IEEE Asia Pacific Board.

Eiji Oki (M'95) received the B.E. and M.E. degrees in instrumentation engineering and the Ph.D. degree in electrical engineering, all from Keio University, Yokohama, Japan, in 1991, 1993, and 1999, respectively.

In 1993, he joined the Communication Switching Laboratories, Nippon Telegraph and Telephone Corporation's (NTT), Tokyo, Japan. He has been researching multimedia-communication network architectures based on ATM techniques and traffic-control methods for ATM networks. He is now engaged in researching and developing high-speed switching systems. He is currently a Visiting Scholar at Polytechnic University, Brooklyn, NY, since 2000.

Dr. Oki received the Switching System Research Award and the Excellent Paper Award from the IEICE, in 1998 and 1999, respectively. He is a member of the IEICE of Japan.

Seisho Yasukawa (M'99) received the B.E. and M.E. degrees from the University of Tokyo, Tokyo, Japan, in 1993 and 1995, respectively.

In 1995, he joined the Network Service Systems Laboratories, Nippon Telegraph and Telephone Corporation (NTT), Tokyo, where he was engaged in research and development of high-speed switching systems. He is currently researching future mobile IP network and multimedia communication network architectures.

Mr. Yasukawa received the IEICE Switching System Research Award in 1999. He is a member of the IEEE Communication Soceity.

Katsuhiko Okazaki was born in Tokyo, Japan, on November 27, 1969. He received the B.E. and M.E. degrees from the University of Electro-communications, Japan, in 1993 and 1995, respectively.

In 1995, he joined the Network Service Systems Laboratories, Nippon Telegraph and Telephone Corporation (NTT), Tokyo. He has been researching high-speed and high-density packaging technologies for large capacity ATM switching systems. He is currently developing multiservice node systems.

Mr. Okazaki is a member of the IEICE of Japan, JIEP, and IMAPS.

Akira Ohki was born in Saitama, Japan, on November 30, 1961. He received the B.E., M.E., and Ph.D. degrees in electrical engineering from Nagoya University, Japan, in 1984, 1986, and 1994, respectively.

In 1986, he joined NTT Ibaraki Electrical Communication Laboratories, Ibaraki, where he engaged in research on MOVPE growth of II–VI compound materials. In 1993, he moved to NTT Opto-Electronics Laboratories, Atsugi City, Japan, where he engaged in research on blue-green laser diodes based on ZnMgSSe quaternary alloy crystals. Since 1997, he has been engaged in the development of parallel optical interconnection modules. He is presently a Senior Research Engineer at NTT Photonics Laboratories.

Dr. Ohki is a member of the Institute of Electronics, Information, and Communication Engineers of Japan and the Japan Society of Applied Physics.

Mitsuo Usui was born in Nagano, Japan, on August 31, 1965. He received the B.E. and M.E. degrees from Tokyo Denki University, Tokyo, Japan, in 1988 and 1990, respectively.

In 1990, he joined Nippon Telegraph and Telephone (NTT) Corporation, Kanagawa, Japan. Since then, he has been engaged in research on packaging technology for electronic and optoelectronic components, including optoelectronic multichip modules (OE-MCM), polymeric optical waveguides, and multiport optical connectors for optical interconnection use. He is presently with NTT-ME Corporation.

Mr. Usui received the Young Engineer Award from IEICE in 1997 and the Best Paper Award and the Inose Award from IEICE in 2000. He is a member of the Institute of Electronics, Information, and Communication Engineers of Japan (IEICE) and the Japan Society of Applied Physics.

Nobuo Sato was born in Tokyo, Japan, on January 22, 1952. He received the B.S. degree from the Science University of Tokyo, in 1977.

In 1970, he joined NTT Electrical Communications Laboratories, Musashino, Japan, where he was engaged in research on electron exposure systems and microwave packaging for GaAs MMICs. Since 1996, he has been a Senior Research Engineer. He is currently working on parallel optical interconnection module packaging for future communication systems at NTT Opto-electronics Laboratories.

Mr. Sato is a member of the Japan Society of Applied Physics.

Kosuke Katsura (M'91) was born in Hyogo, Japan, on March 15, 1956. He received the B.E. and M. E. degrees in electrocommunication engineering from the University of Electrocommunications, Tokyo, Japan, in 1979 and 1981, respectively.

He joined the NTT Electrical Communication Laboratories, Kanagawa, Japan, in 1981 and has been engaged in the research and development of packaging technology for electronic and optoelectronic components, including interconnection and casing techniques for high-speed modules. Currently, he is responsible for the development of parallel optical interconnections.

Mr. Katsura received the Excellent Paper and Inose Awards from the IEICE. He is a member of the Institute of Electronics, Information, and Communication Engineers of Japan (IEICE), and the IEEE Components, Packaging, and Manufacturing Technology Society and Lasers Electro-Optics Society.

Yasuhiro Ando (M'90–SM'99) was born in Kobe, Japan, on June 4, 1951. He received the B.S. and M.S. degrees in electronics engineering from Osaka University, Japan, in l974 and l976, respectively.

Since joining NTT Electrical Communications Laboratories, Kanagawa, Japan, in l976 he has been engaged in research on electrical contact and optical connection technologies, and in the development of electrical/optical connectors for advanced digital communication systems. He is currently directing a project on optical interconnection and systems packaging technology. He is now Senior Research Engineer, Supervisor, and Photonic Interconnection Research Group Leader of NTT Telecommunications Energy Laboratories, Atsugi, Japan. He was Advisory Member of the IEICE TRANSACTIONS ON ELECTRONICS, from 1998 to 2000.

Mr. Ando received the MOC Paper Award from the Microoptics Conference, in 1999, the Electronics Society Award in 1999 from the IEICE Electronics Society, and the Excellent Paper and Inose Awards from the IEICE in 1999. He is a member of the Institute of Electronics, Information, and Communication Engineers (IEICE) of Japan, and was a Chairperson of the Technical Group on Electromechanical Devices. He has been serving as a Co-Chairman of the Technical Program Committees of the IEEE Electronic Components and Technology Conference (ECTC) and the International Electronic Manufacturing Technology and International Microelectronics Conference (IEMT/IMC) Symposium. He has also been serving for standardization of optical link modules as a Member of TC86/SC86C/WG1 and WG4 at International Electrotechnical Commission (IEC).

Toshiaki Kagawa was born in Kanagawa, Japan, on October 22, 1952. He received the B.S., M.S., and Ph.D. degrees in physics from Tokyo Institute of Technology, Tokyo, Japan, in 1975, 1977, and 1985, respectively.

In 1977, he joined NTT. He has engaged in research and development of amorphous semiconductor, superlattice avalanche photodiodes, and vertical cavity surface emitting laser diodes. He was a Visiting Scientist at the Max-Planck-Institute, Germany, from 1993 to 1994.

Dr. Kagawa is a member of the Japan Society of Applied Physics, and the Institute of Electronics, Information, and Communication Engineers of Japan.

Makoto Hikita (M'98) was born in Tokyo, Japan, in 1950. He received the B.E. and M.E. degrees in instrumentation engineering from Keio University, Japan, in 1973 and 1975, respectively, and the Ph.D. degree in physics from Osaka University, Japan, in 1990.

In 1975, he joined NTT Musashino Laboratories, Tokyo, where he was engaged in research on superconducting telecommunication cables. In 1980, he moved to NTT Ibaraki Laboratories where he was engaged in research on superconducting materials, Josephson devices, Anderson localization, and superconducting physics. Since 1992, he has been engaged in the development of electrooptic and passive polymer optical component devices. In 2000, he moved to NTT Advanced Technology Corporation (NTT-AT), Kanagawa, Japan. He is a Senior Engineer at NTT-AT.

Dr. Hikita is a member of The Institute of Electronics, Information, and Communication Engineers of Japan, The Physical Society of Japan, The Society of Polymer Science of Japan, The Japan Society of Applied Physics, Japan Institute of Electronics Packaging and IEEE/LEOS.