

The following conclusions are obtained. The path lengths of the parts and the robot increase with increasing task complexity. This can be attributed to two factors: first, the closer the parts need to be packed together, the more careful and precise the robot has to be in its movements; secondly, as there is an increased possibility of collision with the parts, there is more dodging around. Interestingly, compared to simulations, the paths taken by the parts are only 10% longer on average (Fig. 3). As expected, path lengths in real experiments tend to vary more owing to the sensor inaccuracies and non-ideal motion capabilities of the robot. The positional inaccuracies in experiments range between 2.0–5.3 cm/part. In simulations we observe much lower inaccuracies which we attribute again to the EDAR sensor and actuator hardware limitations and not to our approach.

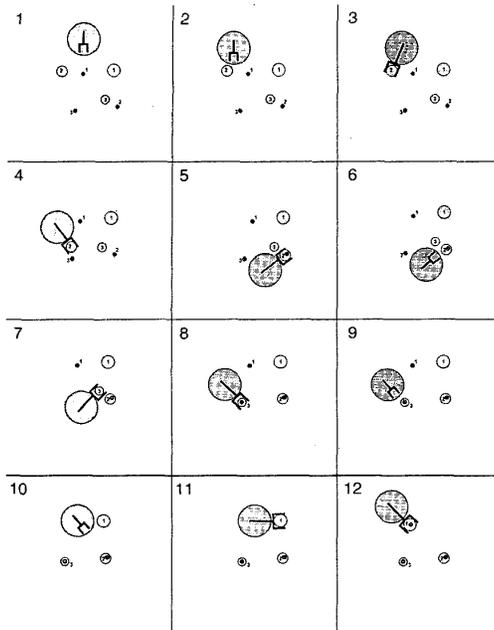


Fig. 2 Snapshots of experiment with three parts

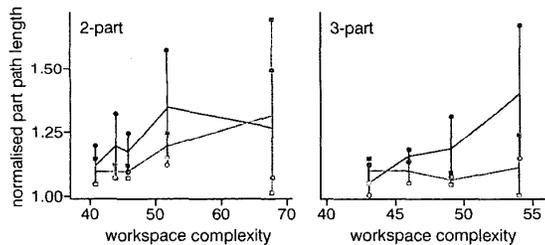


Fig. 3 Part path length statistics against workspace complexity

■ □ Simulation data  
● ○ Experimental data

These experiments serve to demonstrate that EDAR can successfully complete parts moving tasks, using a purely event-driven strategy.

*Acknowledgments:* This work is supported by NSF-TÜBİTAK INT9819890 and TÜBİTAK MİSAG65.

© IEE 2002

Electronics Letters Online No: 20020089  
DOI: 10.1049/el:20020089

C.S. Karagöz and H.I. Bozma (Department of Electrical and Electronic Engineering, Intelligent Systems Laboratory, Boğazii University, Istanbul, Turkey)

E-mail: karagose@boun.edu.tr

D.E. Koditschek (EECS Department, Artificial Intelligence Laboratory, College of Engineering, University of Michigan, Ann Arbor, MI, USA)

14 October 2001

## References

- 1 LATOMBE, J.-C.: 'Robot motion planning' (Kluwer, Boston, MA, USA, 1991)
- 2 CHA, Y.Y., and GWEON, D.G.: 'Local path planning of a free ranging mobile robot using the directional weighting method', *Mechatronics*, 1996, **6**, (1), pp. 53–80
- 3 NOREILS, F., and CHATILA, R.G.: 'Plan execution, monitoring and control architecture for mobile robots', *IEEE Trans. Robot. Autom.*, 1995, **11**, (2), pp. 255–266
- 4 KODITSCHKEK, D.E.: 'Task encoding: toward a scientific paradigm for robot planning and control', *Robot. Auton. Syst.*, 1992, **9**, pp. 5–39
- 5 RIMON, E., and KODITSCHKEK, D.E.: 'Exact robot navigation using artificial potential functions', *IEEE Trans. Robot. Autom.*, 1992, **8**, (5), pp. 501–518
- 6 BOZMA, H.I., and KODITSCHKEK, D.E.: 'Assembly as a noncooperative game of its pieces: analysis of 1D sphere analysis', *Robotica*, 2001, **19**, pp. 93–108

## Dynamic deficit round-robin scheduling scheme for variable-length packets

K. Yamakoshi, K. Nakai, E. Oki and N. Yamanaka

A dynamic deficit round-robin (DDRR) scheduling scheme for variable-length packets is proposed. It can resolve the drawback of the conventional deficit round-robin (DRR) scheduler that short-packet delay performance and high throughput cannot be satisfied simultaneously. DDRR uses an adaptive granularity for the deficit counter, where the granularity is dynamically changed according to packet lengths in queues. The algorithm, along with the simulation results showing the efficiency, are presented. The DDRR scheduler was implemented for 5 Tbit/s switching system.

*Introduction:* A fair scheduler for variable-length packets is needed to provide a best-effort Internet-Protocol (IP) service. The deficit round-robin (DRR) [1] scheduling scheme is widely used because of its simplicity to provide the max-min fair share for the best-effort traffic.

However, the DRR scheme cannot satisfy both short-packet delay performance and high throughput, since only a fixed granularity for the deficit counter is allowed. When the granularity is set at too large a value, the short packets are delayed significantly by the long packets. The short-packet delay degradation affects the quality of real-time services such as VoIP. Conversely, the throughput becomes low for a small granularity since the timing margin for the DRR scheduler to satisfy the line speed is reduced as the granularity becomes small.

In this Letter we propose a dynamic deficit round-robin (DDRR) scheduling scheme for variable-length packets. It dynamically changes the granularity for the deficit counter in the scheduler. Simulation results showing the efficiency of the scheduler are presented.

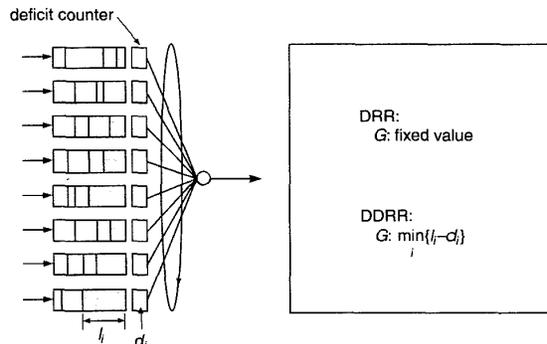


Fig. 1 DRR-based scheduler for eight queues

*Packet scheduling technique:* Fig. 1 is a schematic diagram of a DRR-based scheduler. Fig. 2 shows the average packet-delay dependency on packet length in the case of DRR with the granularity ( $G$ ) of 5, 10, and 100 cells. Here we assumed that the packet length was normalised to an integer number of fixed-size cell times. The length of

arriving packets was assumed to have an exponential distribution with an average length of 10 cells. The probability of packet arrival was assumed to have a Poisson distribution. The short packets are delayed as the granularity becomes large ( $G = 100$ ). It is necessary to use a small granularity ( $G \leq 10$ ) to suppress the short packet delay. However, the work of DRR remains  $O(1)$ , only if  $G$  is greater than the maximum packet length [1]. The number of hops traversing queues needed to decide the output queue is likely to become large as the granularity becomes small, as shown in Fig. 3. For  $G = 10$ , the number of hops happens to be greater than one. The average and maximum value are 1.43 and 6, respectively. This causes the throughput to become low, since there is an upper limit of the hop number at a given line speed. If  $G$  is set to more than 50 cells, the number of hops is exactly one. However, the short packets have a larger delay than the long packets, as shown in Fig. 2.

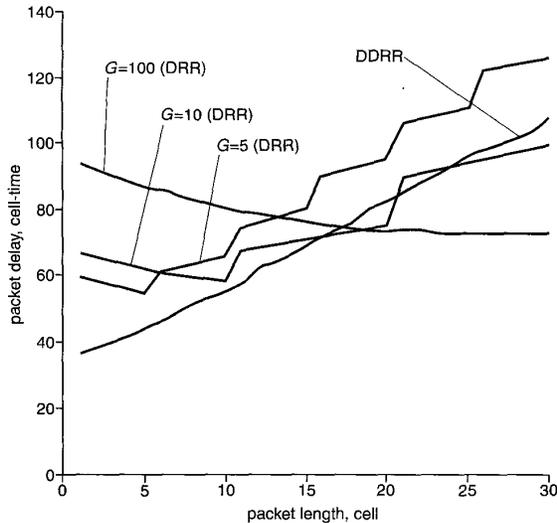


Fig. 2 Packet delay dependency on packet length  
Queues = 8, offered load = 0.95

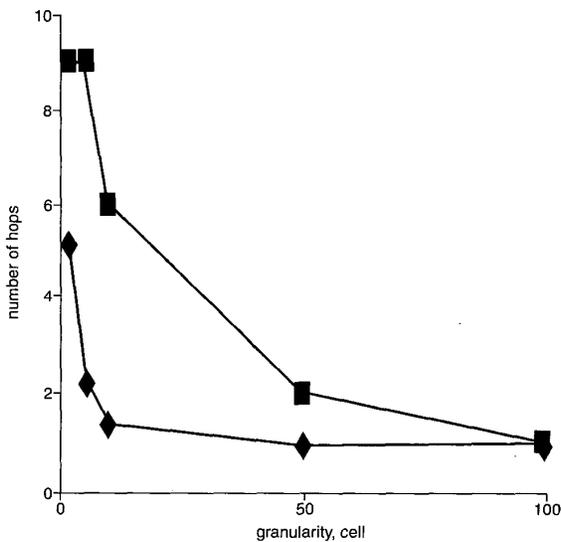


Fig. 3 Number of hops in DRR  
—◆— average  
—■— maximum

To resolve the above drawback, we present a dynamic deficit round-robin (DDRR) scheduling scheme that dynamically changes the granularity for the deficit counter according to the packet lengths at the heads of queues. The DDRR algorithm is as follows.

Step 1. Calculate the difference  $m_i = l_i - d_i$ , where  $l_i$  and  $d_i$  are the packet length at the head of the queue in channel  $i$  ( $1 \leq i \leq N$ ) and the counter value for the channel, respectively.

Step 2. Determine the minimum value  $m_0$  from  $m_i$ .

Step 3. Add the minimum value  $m_0$  to the counters of each channel other than the selected channel.

All  $d_i$ s are set to 0 as the initial condition. In Step 1,  $m_i$  is calculated only when there is a packet at the head of the queue in channel  $i$ . Three steps must be performed within one packet-time in order to meet the line speed. When the number of channels is  $N$ ,  $\log_2 N$  operations determining the smaller of two values  $m_i, m_j$  are required to decide  $m_0$  in Step 2. This relieves the timing margin bottleneck of DRR with small granularity ( $G \leq 10$ ). As Fig. 2 shows, packet delay decreases linearly with decreasing packet length in DDRR. Moreover, the delays of packets shorter than 15 cells were smaller than that in DRR for any value of granularity. Therefore, DDRR can satisfy both high throughput and small delay requirements for short packets, especially under a heavy load. Note that since DDRR is based on DRR, DDRR also provides the max-min fair share independent of packet length. DDRR was used as the scheduler for an experimental 5 Tbit/s switching system [2, 3].

Conclusion: A DDRR scheduling scheme is proposed to resolve a drawback of the DRR scheme. The granularity for the deficit counter of DDRR is adaptively changed according to the packet lengths at the heads of the queues. Simulation results show that DDRR can reduce the delay for short packets while keeping the throughput high.

© IEE 2002

1 November 2001

Electronics Letters Online No: 20020079

DOI: 10.1049/el:20020079

K. Yamakoshi and K. Nakai (NTT Network Service Systems Laboratories, 3-9-11, Midori-Cho, Musashino-shi, Tokyo 185-8585, Japan)

E-mail: yamakoshi.kimihiro@lab.ntt.co.jp

E. Oki and N. Yamanaka (NTT Network Innovation Laboratories, 3-9-11, Midori-Cho, Musashino-shi, Tokyo 185-8585, Japan)

#### References

- SHREEDHAR, M., and VARGHESE, G.: 'Efficient fair queuing using deficit round-robin', *IEEE/ACM Trans. Netw.*, 1996, 4, (3), pp. 375-385
- NAKAI, K., OKI, E., and YAMANAKA, N.: 'Scalable 3-stage ATM switch architecture using optical WDM grouped links based on dynamic bandwidth sharing', *IEICE Trans. Commun.*, 1999, E82-B, (2), pp. 265-270
- YAMAKOSHI, K., NAKAI, K., MATSUURA, N., OKI, E., KAWANO, R., and YAMANAKA, N.: '5-Tbit/s frame-based ATM switching system using 2.5-Gbit/s  $\times$  8 optical WDM links'. Proc. IEEE ICC'01, pp. 3117-3121