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A Dynamic Reference Single-Ended ECL Input Interface Circuit for MCM-Based 80-Gbps ATM Switch

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SUMMARY A high-speed dynamic reference single-ended ECL input-interface circuit has been fabricated for advanced ATM switching MCMs. To raise the limit on the number of I/O pins, this circuit operates with a reference signal directly generated from the input signal itself. The reference level is changed dynamically to achieve a larger noise margin for operation. Experimental results show that operation up to 3.4 Gbps with a large level margin can be attained. We deploy this circuit to the input interface LSIs of an 80-Gbps ATM switching MCM.

key words: *MCM, ECL interface, high-speed interconnection, noise margin*

1. Introduction

The growing volume of multimedia communication traffic means that asynchronous transfer mode (ATM) switching systems capable of Tbps-class throughput will be required, and several such systems are under study [1], [2]. The progress in reducing the CMOS process rule means that switches with throughput from about 10 to 40 Gbps will be attainable with a single chip CMOS LSI [3].

However, despite the performance improvement of the LSI itself, the I/O interface throughput has become a bottleneck in its assembly technology. Therefore, even if the LSI I/O speed rises to around to the Gbps level, it will be very difficult to handle 40-Gbps throughput I/O signals with available packaging and board assembly technology. This is a barrier to the expansion of ATM switch throughput. In large-capacity switching systems, large-scale multi-chip modules (MCMs) will be used because MCMs enable several LSI functions to be concentrated in a single module, reducing the signal interconnection length between LSIs and eliminating packaging [4]. However, in such high-performance MCMs, the I/O throughput is also a severe limitation on further enhancement of performance for the same reason as mentioned above for LSIs.

Comparing the two most popular types of high-speed MCM I/O interfaces, the balanced emitter coupled logic (ECL) (differential type) interface can increase the noise margin and transmit high-speed signals but needs an I/O interface occupying twice the area of that for the unbalanced ECL (single-ended type). So the high-performance MCM I/O throughput for an MCM of a given size is limited by the I/O pin area when using the differential type. On the other hand, the single-ended type is not resistant to noise.

For these reasons, we have developed a single-ended-type input interface circuit with a wide noise margin to improve the MCM I/O throughput. We implemented an MCM interface LSI using this circuit and experimentally confirmed operation at up to 3.4 Gbps.

We also describe an 80-Gbps high-speed ATM switch MCM [5], [6] that uses the proposed circuit and LSI. The size of the MCM is 160 mm × 114 mm. This ATM switch MCM has very-large throughput because that of a commercial level ATM switch unit is about 10 to 40 Gbps. To our knowledge, this ATM switch MCM has the highest throughput in one module of that size.

2. High-Speed ATM Switch and MCM I/O

2.1 MCM-Based High-Performance ATM Switch

An ATM switch throughput is defined as the product of highway speed and the number of ports. We have been advancing the input/output buffering type ATM switch architecture shown in Fig. 1. Switch size can be expanded using a cross-bar type architecture. To enhance system packaging efficiency, a hierarchical structure is used in the VLSI, MCM and mother board. A switch element can be expanded to get higher throughput by arranging it in the form of matrix as shown in Fig. 1. The ATM cell having destination address at the cell header routed by address filter, AF. The VLSI has expanding input/output port to easy to expand the switch size.

In this way, we have developed an 80-Gbps MCM-based ATM switch using 0.25 μm CMOS, which has over 500 signal I/Os, each with a speed of 625 Mbps [7]. Due to the development of quarter-micron CMOS technology, the progress in I/O speed, clock speed, and gate number of LSIs has been remarkable. An I/O speed of 2.6 Gbps/pin was made using a pseudo-ECL (PECL) interface circuit [3], [8]. However, LSI packaging technology has not yet caught up with LSI performance and cannot handle several hundred pins and several hundred Mbps signal I/Os concurrently. Therefore, we used 40-

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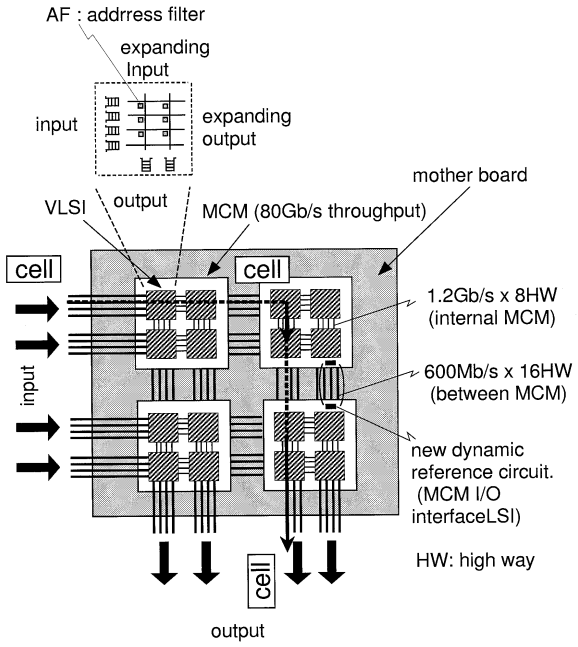

Fig. 1 Large ATM switching system configuration.

layer ceramic MCM technology to eliminate the packaging. Details are described in Sect. 4.

2.2 MCM I/O Interface

In developing an MCM I/O interface LSI with 625-Mbps I/O interface circuits to break through the LSI pin count limit, it is not desirable to use a balanced ECL interface (differential input interface circuit) because it needs twice as many I/O pins as an unbalanced one (single-ended input interface circuit). However, the conventional single-ended type has a poor noise margin in high-speed operation. In a single-ended input interface circuit, the relationship between the input signal and the reference voltage level is important because distortion of the input waveform due to crosstalk or signal reflection can cause errors, as shown in Fig. 2. Changes in reference level due to power fluctuations or manufacturing deviations of the device parameter increase the likelihood of such errors. Here we propose a dynamic reference ECL (DRECL) input interface circuit that has a large noise margin despite being single-ended. In other words, this DRECL has the advantages of both the differential ECL and the single-ended ECL.

3. Dynamic Reference ECL Circuit Design

The DRECL input interface circuit is shown in Fig. 3. The collector node of transistor Q1 generates a reverse phase signal to input signal V_{in}, and the level is shifted by transistor Q2 and input to the base node of transistor Q3 as a dynamic reference level. The reference signal amplitude and offset level can be designed independently by resistors R2/R3 and R1 respectively. The capacitance is only used to smooth QB, and so is not an essential requirement. A simulated waveform of this circuit at 600 Mbps is shown in Fig. 4. Unlike the conventional single-ended ECL input circuit, the reference signal is generated directly by the input signal and its phase is opposite to that of the input signal, so the circuit has a wide noise margin and is resistant to waveform distortion and power voltage fluctuation.

An input circuit with hysteresis input characteristics can improve the noise margin. For example, a Schmitt circuit [9] improves the noise margin by using two voltage thresholds: a high threshold to switch the circuit during low-to-high transitions and a lower threshold to switch the circuit during high-to-low transitions. Such a trigger scheme is immune to noise as long as the peak-to-peak amplitude of the noise is less than the difference between the threshold voltages.

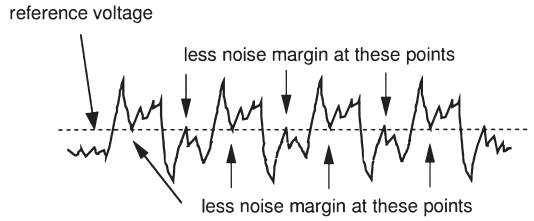

Fig. 2 Drawback of conventional single-ended ECL.

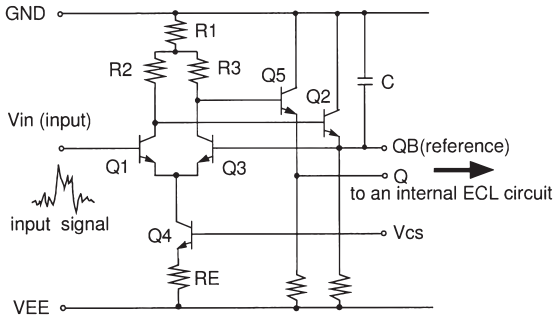

Fig. 3 Schematic diagram of DRECL.

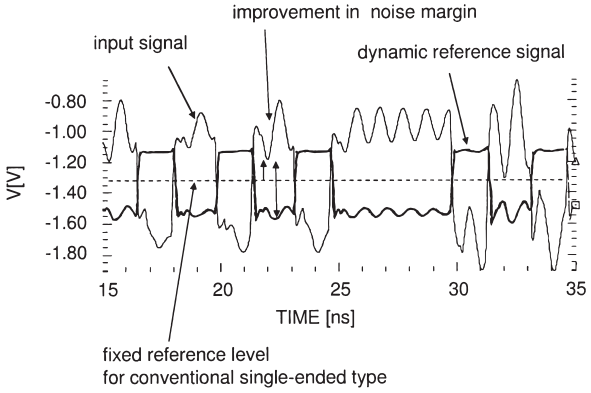

Fig. 4 Simulated waveform of DRECL (600 Mbps).

The DRECL also has two thresholds; that is, the dynamic reference signal in Fig. 4 has both low-level and high-level thresholds. The strong point of the proposed DRECL is its ease of design. The high level, low level, and amplitude of output Q in Fig. 3 is calculated as shown in Eqs. (1), (2), and (3), respectively. The output amplitude and the levels of the DRECL can be designed individually as shown in the equations. Moreover, the precision of the amplitude and levels is always determined by the ratio between the the resistors in Eqs. (1), (2), and (3). Thus the DRECL is resistant to fabrication deviations in the resistors.

$$V_H = -R_1 \frac{V_{CS} - V_{BE}(Q_4)}{R_E} - V_{BE}(Q_5) \quad (1)$$

$$V_L = -(R_1 + R_3) \frac{V_{CS} - V_{BE}(Q_4)}{R_E} - V_{BE}(Q_5) \quad (2)$$

$$V_H - V_L = R_3 \frac{V_{CS} - V_{BE}(Q_4)}{R_E} \quad (3)$$

4. Experimental Results

4.1 DRECL Circuit Evaluation

A DRECL circuit in packaged form was evaluated in detail. An output waveform given the input of a PN23 pseudo-random bit sequence (PRBS) is shown in Fig. 5. The DRECL circuit operates at up to 3.4 Gbps with PN23 PRBS with a bit error rate (BER) of less than 10^{-9}. The measured error-free operation range of the DRECL input buffer and that of a conventional ECL input buffer at 700 Mbps under the same device process technology, SST-1B are shown in Fig. 6. The evaluated conventional ECL input buffer is of the single-ended type. Here, the input amplitude was 0.3 $V_{p\text{-}p}$ and V_{th} in the figure indicates the center level of each input signal. Here the reference level of the conventional ECL input buffer (V_{BB}) was designed to be -1.3 V, and the designed I/O speed was 625 Mbps. The figure shows that the DRECL input buffer is up to 170% more resistant to fluctuations in input signal level than the conventional one. The reason for its wide operating range is that the DRECL input buffer generates the threshold signal by itself.

4.2 Application to the Interface LSI

We developed a 10-Gbps-throughput input and output interface LSI chip set for an MCM-based 80-Gbps ATM switch to relief the difficulty of the interconnection between the MCMs. The block diagrams of the input and output interface LSIs are shown in Fig. 7 and Fig. 8 respectively. The input interface LSI has functions of 2 : 1 data-multiplexing and clock-speed conversion and 625-Mbps signals are up-converted to 1.25-Gbps signals. In

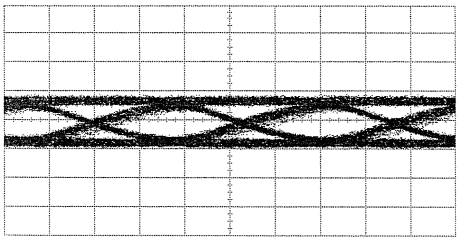

Fig. 5 Experimental waveform of DRECL (3.0 Gbps).

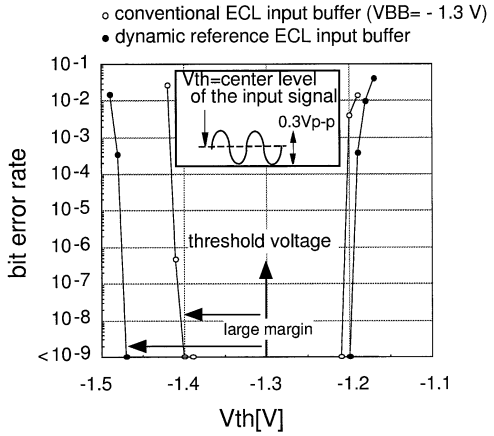

Fig. 6 Bit error rate characteristic of DRECL.

the input interface LSI, clock speed is up-converted. This is done by an EXOR using the original clock and a clock that is delayed by half a period from the original clock. This LSI has 16 data inputs and 8 outputs and DRECL is used in the 16 data input buffers. The main features of the LSI are listed in Table 1. The output interface LSI has functions of 1 : 2 data-demultiplexing and clock-speed conversion and 1.25-Gbps signals are down-converted to 625-Mbps signals. Therefore, this LSI has 8 data inputs and 16 outputs. The main features of the LSI are given in Table 2.

Figure 9 shows a microphotograph of the gate-array-based input interface LSI. The input and output interface LSIs were made using 1.0-μm Si-bipolar super-self-aligned process technology (SST-1B [10]), which can achieve cut-off frequencies of up to 25.7 GHz.

4.3 Constitution of the 80-Gbps MCM

The 80-Gbps MCM consists of 0.25 μm CMOS switching VLSIs and the input and output interface LSIs as shown in Fig. 10. Half of them are used to support the expansion routes. Inside the MCM, we employ a single-ended 1.25-Gbps ECL interface and a pseudo-ECL interface. To suppress the number of I/O signals as small as possible, we used very-high speed I/O interconnection technology in the MCM. The maxi-

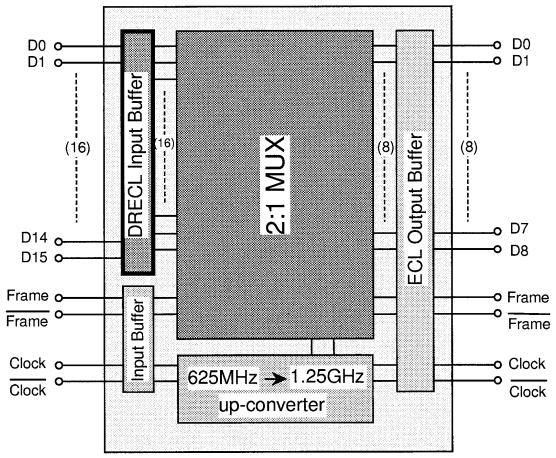

Fig. 7 Block diagram of the input interface LSI.

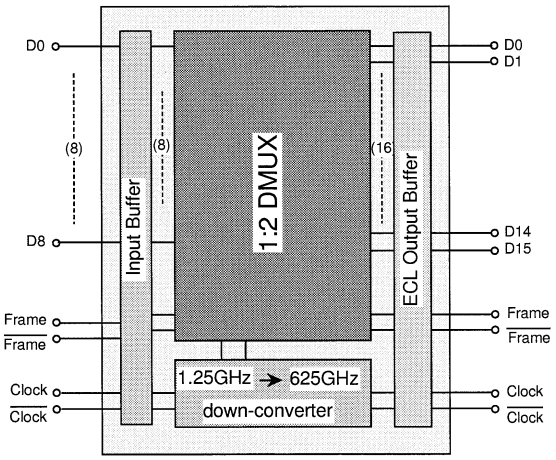

Fig. 8 Block diagram of the output interface LSI.

Table 1 Main features of the intput interface LSI.

throughput	10Gb/s (625Mb/s x 16)	
function	data	625Mb/s → 1.25Gb/s
	CK	625MHz → 1.25GHz
I/O interface	ECL level	
power supply	VEE=-4.5V, VTT=-2V	
power	4.6W	
device process	Si-bipolar (SST-1B)	
chip size	6.5mm x 6.5mm	

Table 2 Main features of the output interface LSI.

throughput	10Gb/s (625Mb/s x 16)	
function	data	1.25Gb/s → 625Mb/s
	CK	1.25GHz → 625MHz
I/O interface	ECL level	
power supply	VEE=-4.5V, VTT=-2V	
power	3.5W	
device process	Si-bipolar (SST-1B)	
chip size	6.5mm x 6.5mm	

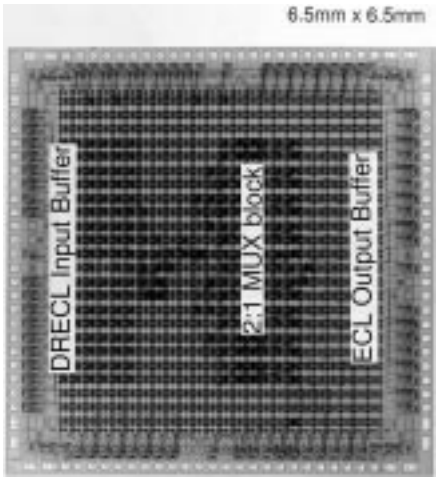

Fig. 9 Microphotograph of the interface LSI.

mum line length is less than 40 mm using a matrix-form-expandable architecture. In other words, only adjustable interconnects with proper operating margin are used. On the other hand, MCMs are linked by a newly developed DRECL circuit. Figure 11 is a cross section of the MCM connection on the Print Wired Board (PWB). The two MCMs are connected by Flexible Printed Circuit (FPC) cable and Flexible Printed Circuit (FPC) connectors. The FPC-cable has 98 contacts with 0.4 mm pitch double-sided tri-plate micro strip line structure [11]. 20 Gb/s data are transmitted via a FPC cable and FPC connector in the MCM. We confirmed the 80-Gbps MCM interface under DRECL operation.

The ATM switch MCM not only has a very-large throughput but also is scalable by using expansion routes. Therefore, the total throughput can be enhanced by connecting the MCMs.

5. Variant of Dynamic Reference Circuit

The dynamic reference circuit offers the advantages of low pin count and high-speed operation. In this section, a variant of the dynamic reference circuit for the low voltage interface circuit is described from the view point of power dissipation. Simulation and basic experimental results are also described.

The LSI with large number of ECL based interface has the disadvantage of large power dissipation for large amplitude and its termination. Thus, the interface part of the 80-Gbps MCM dissipate much power. To realize dynamic reference circuit in a low-power dissipation LSI, we think that non-threshold logic (NTL) [12] is useful because it affords low voltage of about −1.2 V and low power dissipation. NTL is basically superior

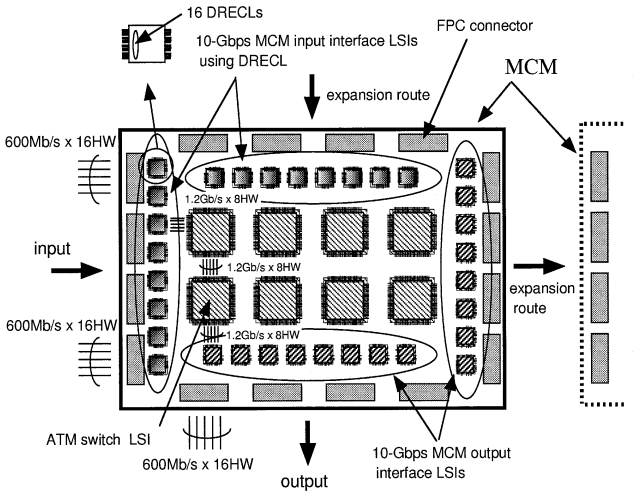

Fig. 10 Configuration of MCM-based 80-Gbps ATM switch.

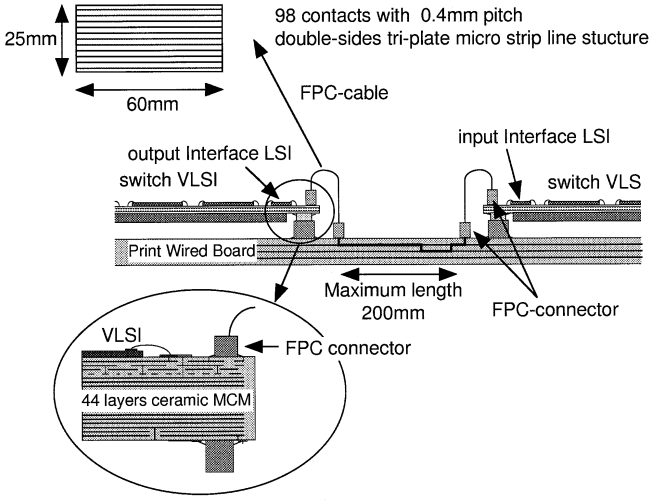

Fig. 11 Cross section of MCM interconnection.

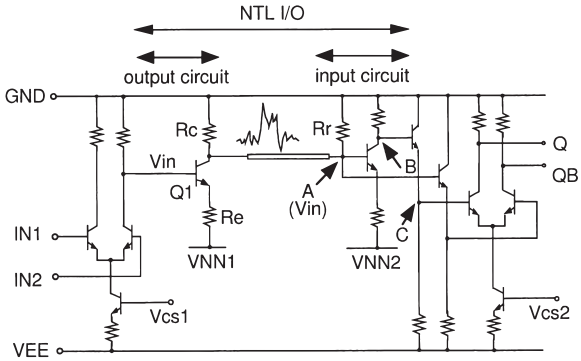

Fig. 12 Schematic diagram of NTL I/O interface.

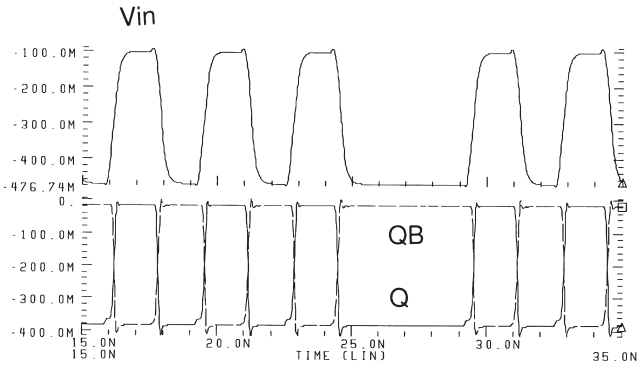

Fig. 13 Simulated waveform of NTL I/O interface (600 Mbps).

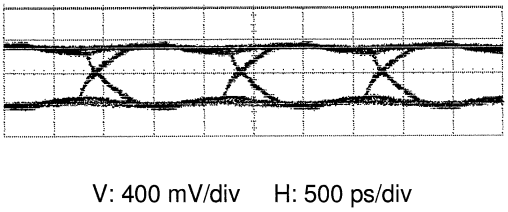

Fig. 14 Experimental waveform of NTL I/O interface (700 Mbps).

to the application of low-power voltage LSI. NTL have been regarded that it has disadvantage of constituting complex logic. However, the application to an I/O buffer circuit does not have the disadvantage, because an I/O buffer circuit is usually simple. We designed a novel interface circuit that combines NTL and ECL, as shown in Fig. 12. The inverter characteristics of the NTL are used to generate the threshold voltage of the ECL circuit. The DRECLs shown in Fig. 4 have positive feedback loops, while the NTL circuit in Fig. 12 operates just as an inverter. The reference voltage of node C in Fig. 12 is changed dynamically by input signal V_{in}, so in a wider sense we can call this scheme a DRECL.

Figure 13 shows a 600-Mbps simulated waveform of the NTL I/O interface circuit. Since the NTL circuit operates as an inverter, nodes A and B have opposing phases. These signals are level-shifted to yield the Q and QB in Fig. 13. This interface circuit does not need a fixed reference level. The experimentally measured 700-Mbps output waveform of dynamic reference circuit with NTL with a PN23 PRBS is shown in Fig. 14. The waveform has good eye-opening.

6. Conclusion

To eliminate the differential ECL input interface circuit, which needs twice the number of connections as the single-ended type, we newly propose a dynamic reference single-ended ECL (DRECL) input-interface circuit that has a large noise margin despite being single-ended. The proposed DRECL circuit has been fabricated and error-free operation up to 3.4-Gbps is experimentally confirmed. The DRECL input buffer is up

to 170% more resistant to fluctuations in input signal level than the conventional one.

An 80-Gbps MCM-based ATM switch element has been implemented by using the DRECL interface circuit to realize very-large I/O throuput within the small interface area. The interface area is located surroundings of the 160 mm × 114 mm MCM. DRECL operation was also confirmed by evaluating an assembled 80-Gbps MCM. The proposed DRECL satisfies the requirements of small I/O area and large noise margin from a very-large throughput MCM.

We have also developed another new input-interface circuit based on NTL as a variant of the original DRECL circuit and its operation was confirmed by experiments. It has the merit of low-power, in addition to the merits of the original DRECL.

We believe that proposed these two single-ended interface circuits are key technologies for very-large throughput MCM interconnection.

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